



RF Power LDMOS Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

These 50 W RF power LDMOS transistors are designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2110 to 2170 MHz.

- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Vdc, $I_{DQ} = 1200$ mA, $P_{out} = 50$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2110 MHz	18.9	29.8	7.2	-34.0	-18
2140 MHz	19.1	29.3	7.1	-34.0	-25
2170 MHz	19.2	28.9	7.0	-34.0	-17

Features

- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Optimized for Doherty Applications
- In Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13-inch Reel.

AFT21S220W02SR3
AFT21S220W02GSR3

2110–2170 MHz, 50 W AVG., 28 V
AIRFAST RF POWER LDMOS
TRANSISTORS

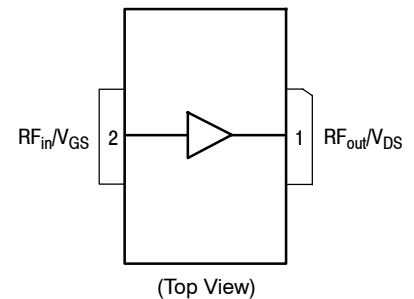
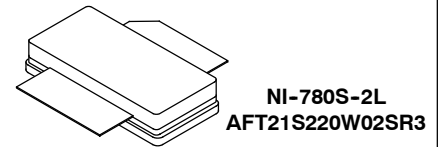


Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	CW	92 0.41	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 91°C , 50 W CW, 28 Vdc, $I_{DQ} = 1200\text{ mA}$, 2140 MHz	$R_{\theta JC}$	0.56	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 300\ \mu\text{Adc}$)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_D = 1200\text{ mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	1.4	1.8	2.2	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 3.0\text{ Adc}$)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

Functional Tests (4,5) (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1200\text{ mA}$, $P_{out} = 50\text{ W Avg.}$, $f = 2140\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.

Power Gain	G_{ps}	18.1	19.1	21.1	dB
Drain Efficiency	η_D	26.0	29.3	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.6	7.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-34.0	-32.0	dBc
Input Return Loss	IRL	—	-25	-12	dB

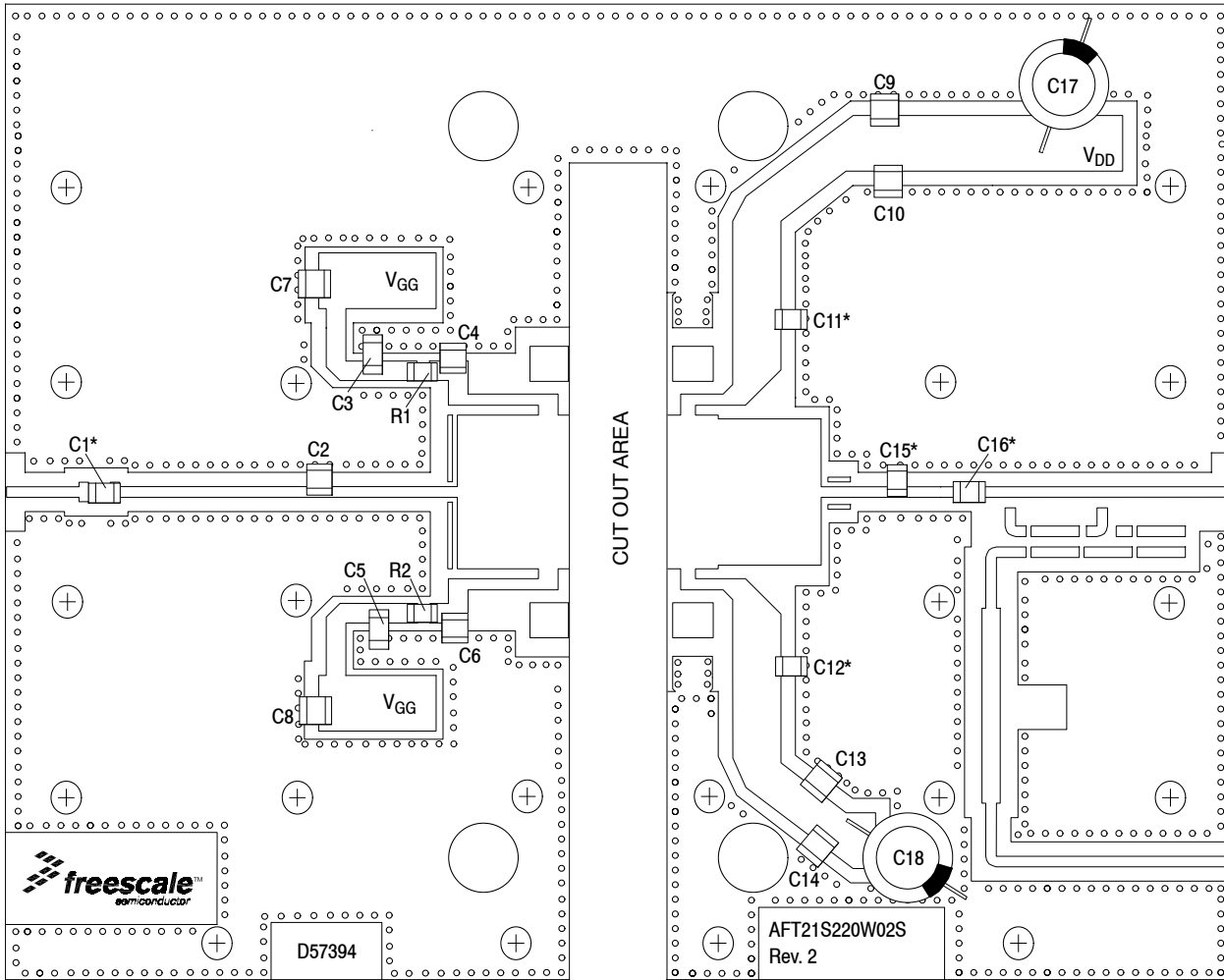
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
4. Part internally matched both on input and output.
5. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GS) parts.

(continued)

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Load Mismatch (In Freescale Test Fixture, 50 ohm system) $I_{DQ} = 1200\text{ mA}$, $f = 2140\text{ MHz}$, 120 μsec Pulse Width, 10% Duty Cycle					
VSWR 10:1 at 30 Vdc, 250 W Pulse Output Power (3 dB Input Overdrive from 180 W Pulse Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1200\text{ mA}$, 2110–2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, 120 μsec Pulse Width, 10% Duty Cycle	P1dB	—	209	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz bandwidth)	Φ	—	-18	—	$^\circ$
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW _{res}	—	80	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 50\text{ W Avg.}$	G_F	—	0.3	—	dB
Gain Variation over Temperature @ 166 W CW (-30°C to +85°C)	ΔG	—	0.02	—	dB/°C
Output Power Variation over Temperature @ 166 W CW (-30°C to +85°C) (1)	$\Delta P1dB$	—	0.01	—	dB/°C

1. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.



*C1, C11, C12, C15 and C16 are mounted vertically.

Figure 2. AFT21S220W02SR3 Test Circuit Component Layout

Table 5. AFT21S220W02SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C4, C6, C11, C12, C16	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C2	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C3, C5	0.1 μ F Chip Capacitors	C1206C104K1RACTU	Kemet
C7, C8, C9, C10, C13, C14	10 μ F Chip Capacitors	GRM32ER61H106KA12L	Murata
C15	2.2 pF Chip Capacitor	ATC100B2R2JT500XT	ATC
C17, C18	470 μ F, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1, R2	4.75 Ω , 1/4 W Chip Resistors	CRCW12064R75FNEA	Vishay
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D57394	MTL

TYPICAL CHARACTERISTICS

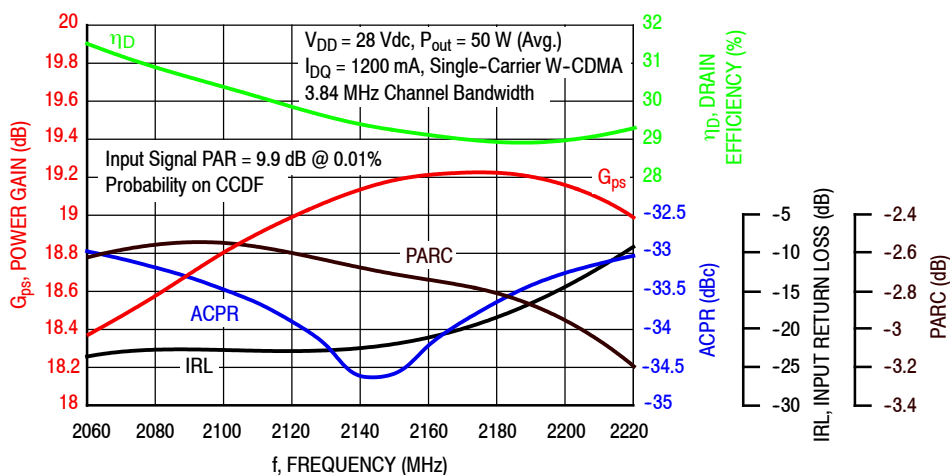


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 50$ Watts Avg.

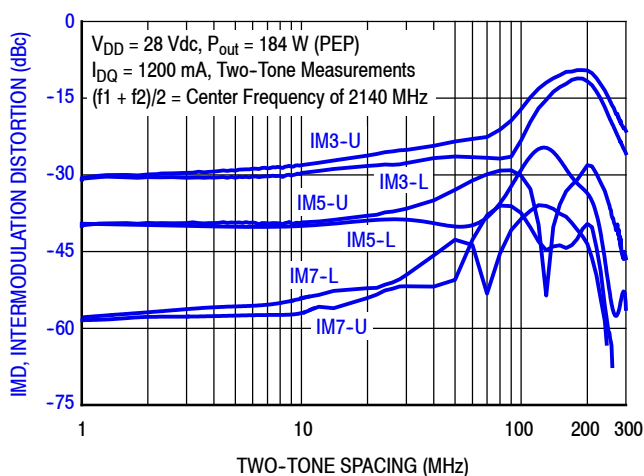


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

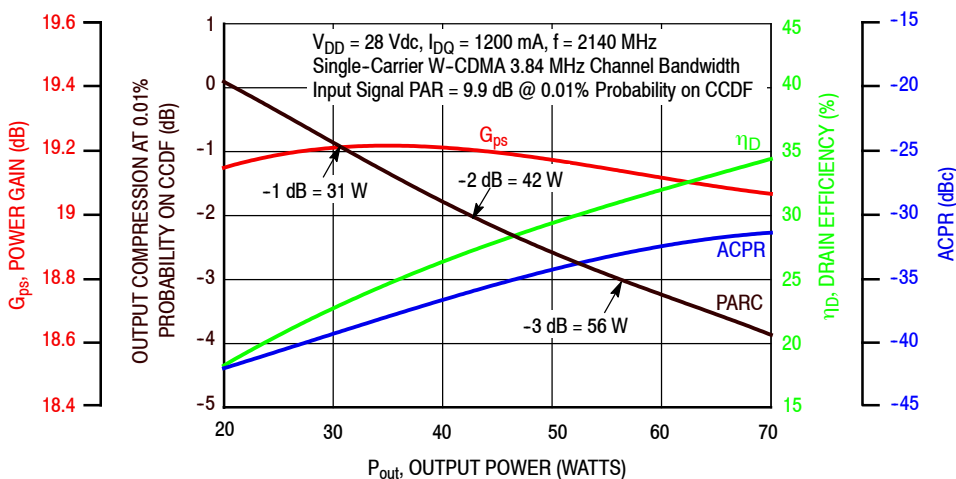


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

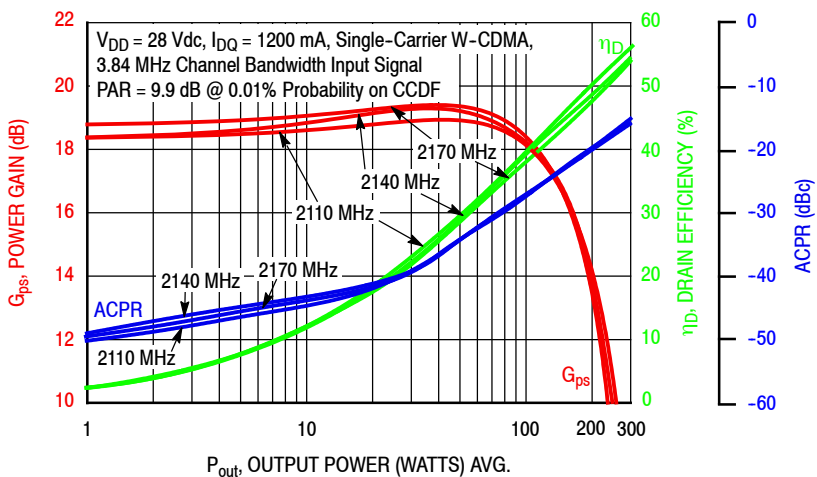


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

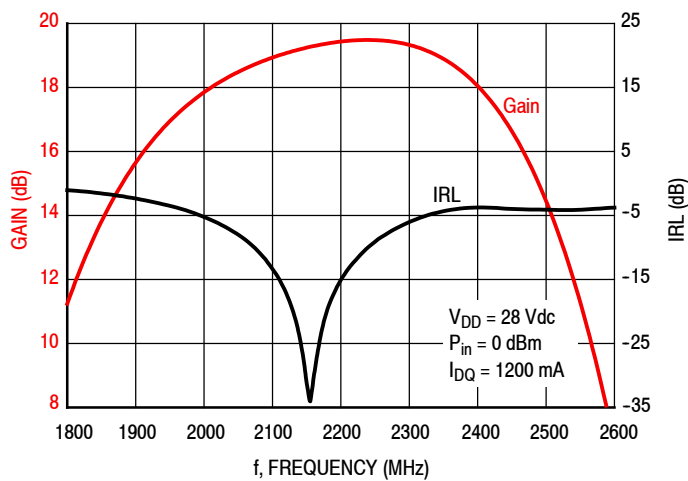


Figure 7. Broadband Frequency Response

Table 6. Load Pull Performance — Maximum Power Tuning

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1260 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec(ON)}$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.03 - j5.49	3.14 + j5.71	3.09 - j5.64	18.8	54.2	264	50.3	-12
2140	3.62 - j5.77	4.06 + j5.98	3.37 - j5.73	18.8	54.1	255	49.0	-12
2170	4.75 - j5.91	5.19 + j5.97	3.49 - j5.61	19.0	54.0	253	49.5	-13

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.03 - j5.49	3.35 + j5.99	3.70 - j6.29	16.6	55.1	322	51.8	-17
2140	3.62 - j5.77	4.42 + j6.26	3.88 - j6.19	16.6	55.0	314	51.0	-18
2170	4.75 - j5.91	5.69 + j6.11	4.28 - j6.16	16.6	54.9	310	50.7	-18

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 7. Load Pull Performance — Maximum Drain Efficiency Tuning

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1260 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec(ON)}$, 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.03 - j5.49	3.17 + j5.81	2.97 - j3.19	20.7	52.9	196	59.1	-18
2140	3.62 - j5.77	4.19 + j6.13	2.59 - j3.06	20.7	52.6	183	58.3	-21
2170	4.75 - j5.91	5.36 + j5.92	2.76 - j3.04	20.8	52.6	183	58.6	-20

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.03 - j5.49	3.32 + j6.09	3.03 - j3.22	18.7	53.7	233	61.4	-27
2140	3.62 - j5.77	4.46 + j6.38	2.64 - j3.06	18.7	53.3	215	60.3	-29
2170	4.75 - j5.91	5.78 + j6.11	2.85 - j3.15	18.7	53.5	222	60.5	-28

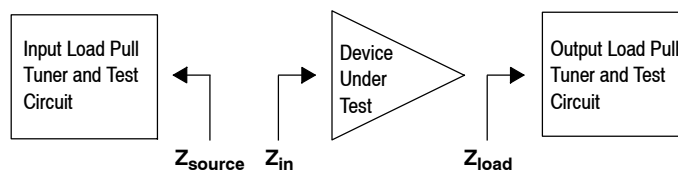
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

Z_{in} = Impedance as measured from gate contact to ground.

Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

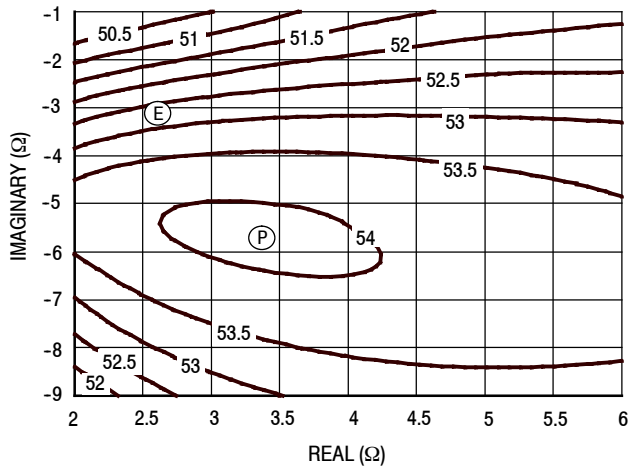


Figure 8. P1dB Load Pull Output Power Contours (dBm)

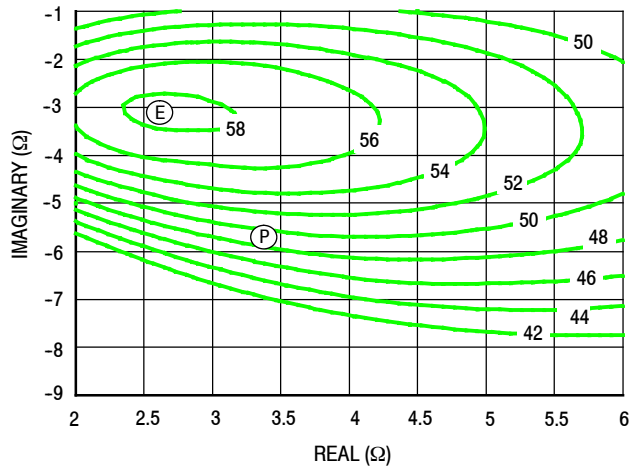


Figure 9. P1dB Load Pull Efficiency Contours (%)

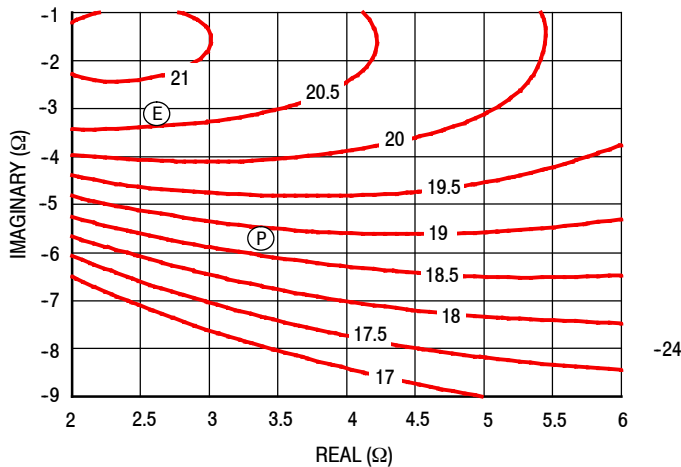


Figure 10. P1dB Load Pull Gain Contours (dB)

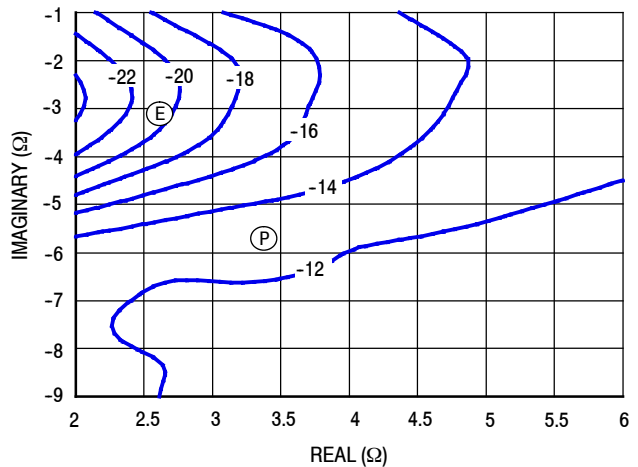


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 2140 MHz

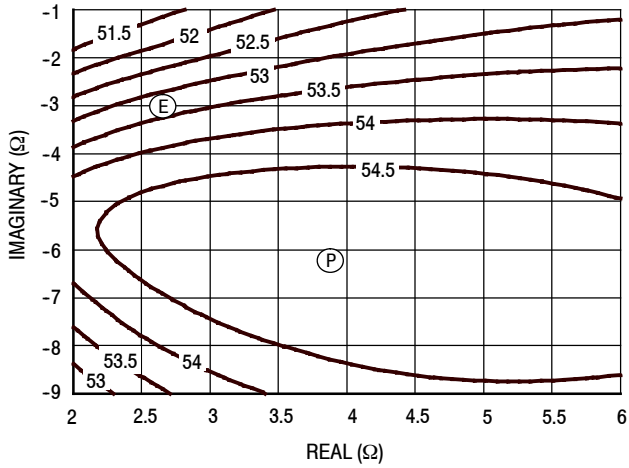


Figure 12. P3dB Load Pull Output Power Contours (dBm)

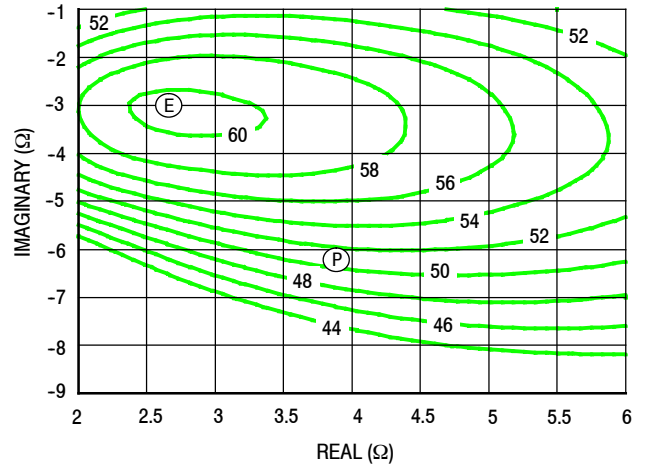


Figure 13. P3dB Load Pull Efficiency Contours (%)

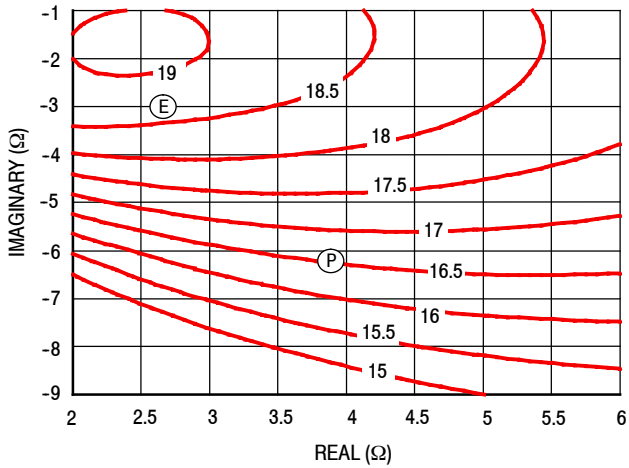


Figure 14. P3dB Load Pull Gain Contours (dB)

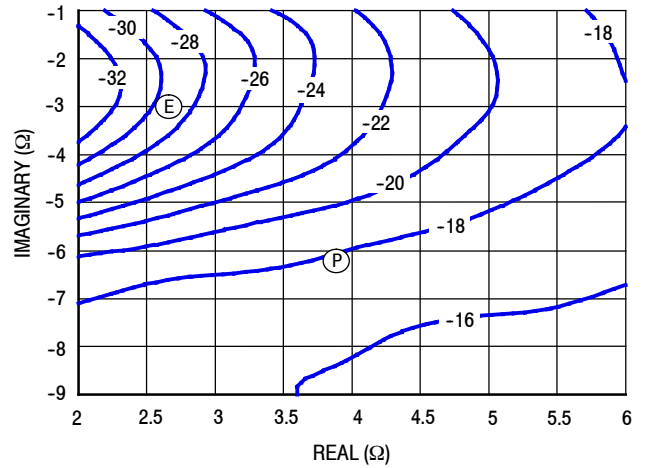
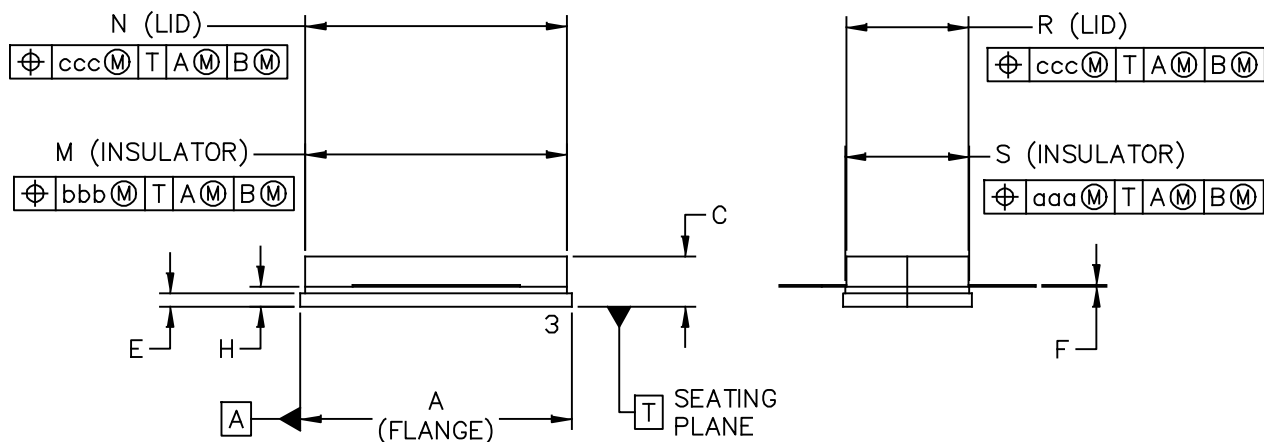
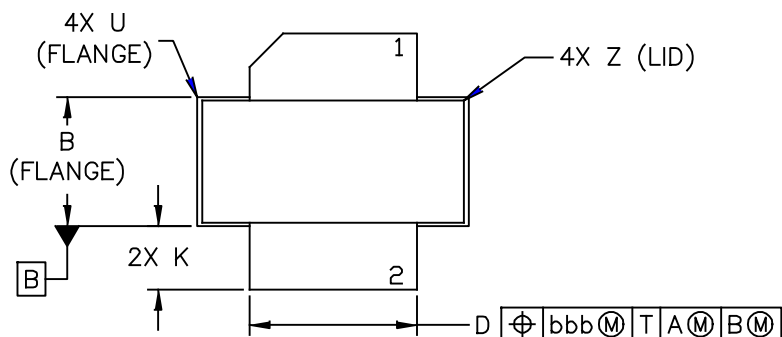


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

PACKAGE DIMENSIONS



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TITLE: NI-780S		DOCUMENT NO: 98ASB16718C		REV: H	
		CASE NUMBER: 465A-06		31 MAR 2005	
		STANDARD: NON-JEDEC			

NOTES:

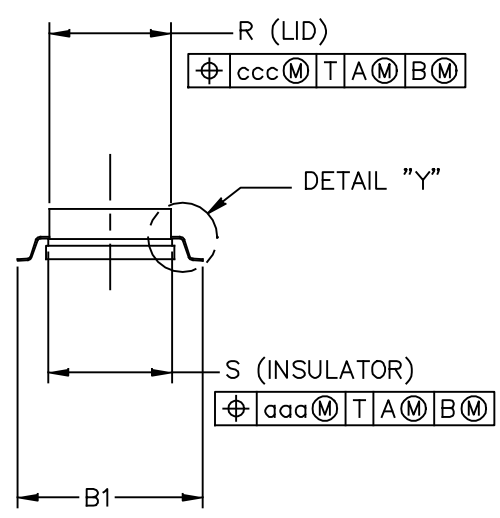
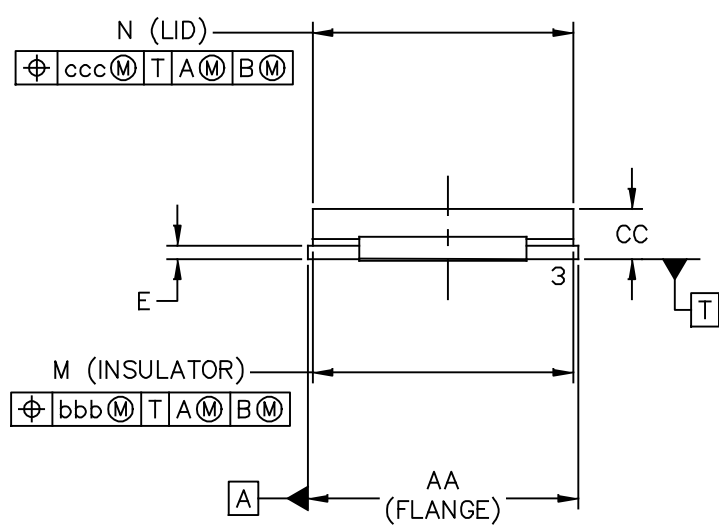
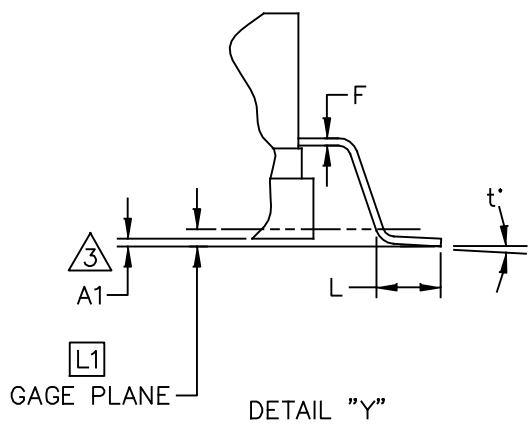
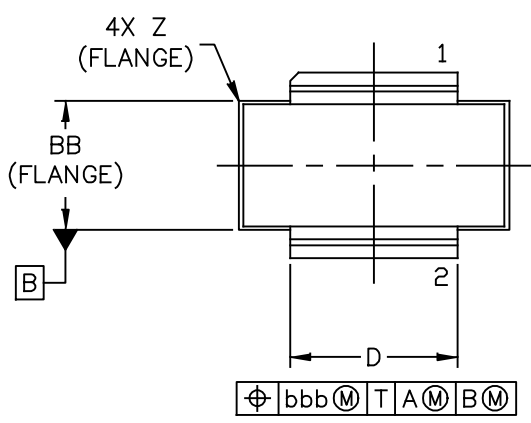
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	-.815	20.45	20.7	U	-.040	-	-	1.02
B	.380	-.390	9.65	9.91	Z	-.030	-	-	0.76
C	.125	-.170	3.18	4.32	aaa	-.005	-	-	0.127
D	.495	-.505	12.57	12.83	bbb	-.010	-	-	0.254
E	.035	-.045	0.89	1.14	ccc	-.015	-	-	0.381
F	.003	-.006	0.08	0.15	-	-	-	-	-
H	.057	-.067	1.45	1.7	-	-	-	-	-
K	.170	-.210	4.32	5.33	-	-	-	-	-
M	.774	-.786	19.61	20.02	-	-	-	-	-
N	.772	-.788	19.61	20.02	-	-	-	-	-
R	.365	-.375	9.27	9.53	-	-	-	-	-
S	.365	-.375	9.27	9.52	-	-	-	-	-

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		CASE NUMBER: 465A-06		31 MAR 2005	
		STANDARD: NON-JEDEC			



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		STANDARD: NON-JEDEC	
		05 SEP 2013	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.

3. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM T. THE POSITIVE VALUE IMPLIES THAT THE PACKAGE BOTTOM IS HIGHER THAN THE LEAD BOTTOM.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.805	.815	20.45	20.70	Z	R.000	R.040	R0.00	R1.02
A1	.002	.008	0.05	0.20	t	0	8	0	8
BB	.380	.390	9.65	9.91					
B1	.546	.562	13.87	14.27					
CC	.125	.170	3.18	4.32	aaa	.005		0.13	
D	.495	.505	12.57	12.83	bbb	.010		0.25	
E	.035	.045	0.89	1.14	ccc	.015		0.38	
F	.003	.006	0.08	0.15					
L	.038	.046	0.97	1.17					
L1	.010 BSC		0.25 BSC						
M	.774	.786	19.66	19.96					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.53					
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NI-780GS-2L					STANDARD: NON-JEDEC				
					05 SEP 2013				

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2014	• Initial Release of Data Sheet

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