

# HOTLink II™ SMPTE Receiver Training Clock

## Features

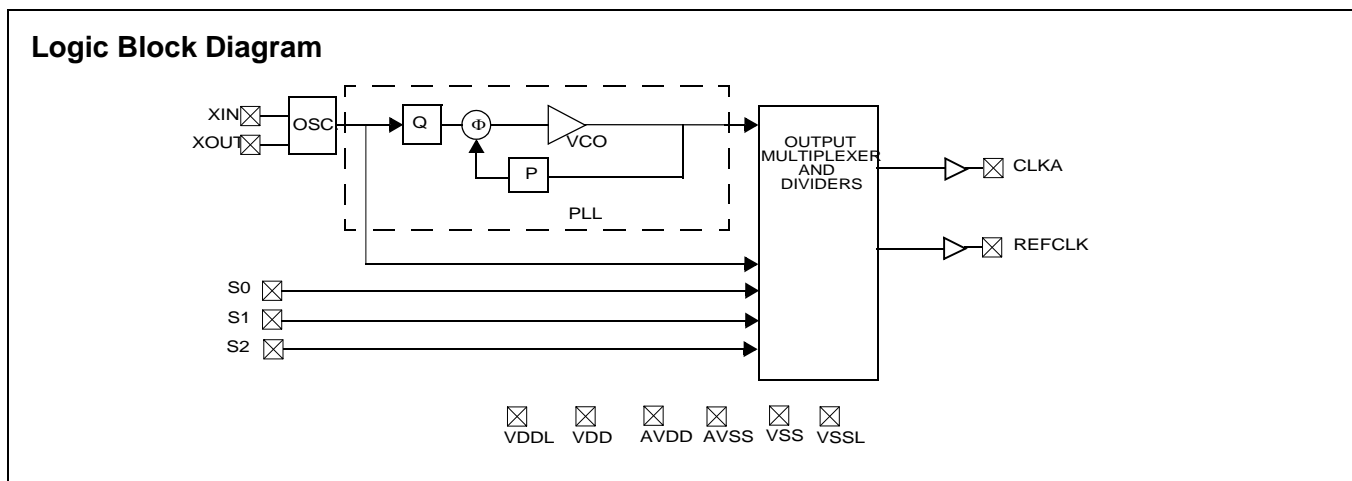
- Integrated phase-locked loop
- Low-jitter, high-accuracy outputs
- 3.3V operation

## Benefits

- Internal PLL with up to 400-MHz internal operation
- Meets critical timing requirements in complex system designs
- Enables application compatibility

**Table 1. Frequency table**

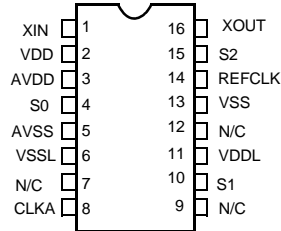
Part Number	Outputs	Input Frequency	Output Frequency Range
CY24130-1	2	27 MHz (Driven Reference)	1 copy 27-MHz reference clock output 1 copy of 27-/36-/54-/148.5-/74.25-MHz (frequency selectable)
CY24130-2	2	27 MHz (Crystal Reference)	1 copy 27-MHz reference clock output 1 copy of 27-/36-/54-/148.5-/74.25-MHz (frequency selectable)



**Table 2. Frequency Select Options**

S2	S1	S0	CLKA	REFCLK	Units
0	0	0	27	27	MHz
0	0	1	36	27	MHz
0	1	0	54	27	MHz
0	1	1	148.50	27	MHz
1	0	0	74.25	27	MHz
1	0	1	OFF, pulled low	27	MHz
1	1	0	OFF, pulled low	27	MHz
1	1	1	OFF, pulled low	27	MHz

## Pin Configuration

**Figure 1. CY24130-1, -2, 16-pin TSSOP**

**Table 3. Pin Definition**

Name	Pin Number	Description
XIN	1	Reference Crystal Input.
V <sub>DD</sub>	2	Voltage Supply.
AV <sub>DD</sub>	3	Analog Voltage Supply.
S0	4	Frequency Select 0.
AV <sub>SS</sub>	5	Analog Ground.
V <sub>SSL</sub>	6	VDDL Ground.
N/C	7	No Connect.
CLKA	8	27-/36-/54-/148.50-/74.25-MHz Clock Output (frequency selectable).
N/C	9	No Connect.
S1	10	Frequency Select 1.
V <sub>DDL</sub>	11	Voltage Supply.
N/C	12	No Connect.
VSS	13	Ground.
REFCLK	14	Reference Clock Output.
S2	15	Frequency Select 2.
XOUT	16	Reference Crystal Output. Leave floating for -1.

## Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V <sub>DD</sub> , AV <sub>DD</sub>	Supply Voltage	-0.5	7.0	V
V <sub>DDL</sub>	I/O Supply Voltage	-	7.0	V
T <sub>J</sub>	Junction Temperature	-	125	°C
	Digital Inputs	AV <sub>SS</sub> - 0.3	AV <sub>DD</sub> + 0.3	V
	Electro-Static Discharge	2	-	kV

## Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub> /AV <sub>DDL</sub> /V <sub>DDL</sub>	Operating Voltage	3.135	3.3	3.465	V
T <sub>A</sub>	Ambient Temperature	0	-	70	°C
C <sub>LOAD</sub>	Max. Load Capacitance	-	-	15	pF
f <sub>REF</sub>	Reference Frequency	-	27	-	MHz
C <sub>LNOM</sub>	Nominal Parallel Crystal Load Capacitance for -2	-	18	-	pF

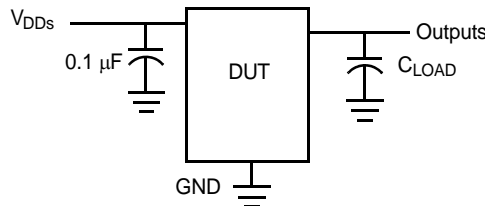
### DC Electrical Specifications

Parameter <sup>[1]</sup>	Name	Description	Min.	Typ.	Max.	Unit
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5, V <sub>DD</sub> /V <sub>DDL</sub> = 3.3V	12	24	-	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.5, V <sub>DD</sub> /V <sub>DDL</sub> = 3.3V	12	24	-	mA
I <sub>IH</sub>	Input High Current	V <sub>IH</sub> = V <sub>DD</sub>	-	5	10	μA
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V	-	-	10	μA
V <sub>IH</sub>	Input High Voltage	CMOS levels, 70% of V <sub>DD</sub>	0.7	-	-	V
V <sub>IL</sub>	Input Low Voltage	CMOS levels, 30% of V <sub>DD</sub>	-	-	0.3	V
I <sub>VDD</sub>	Supply Current	AV <sub>DD</sub> /V <sub>DD</sub> Current	-	16	-	mA
I <sub>VDDL</sub>	Supply Current	V <sub>DDL</sub> Current	-	14	-	mA

### AC Electrical Specifications

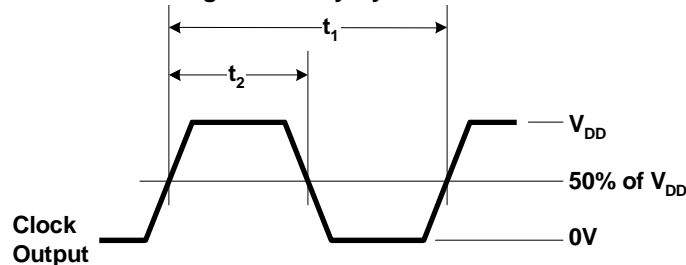
Parameter <sup>[1]</sup>	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 3; t <sub>1</sub> /t <sub>2</sub> , 50% of V <sub>DD</sub>	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V <sub>DD</sub> , C <sub>LOAD</sub> = 15 pF. See Figure 4.	0.8	1.4	-	V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V <sub>DD</sub> , C <sub>LOAD</sub> = 15 pF. See Figure 4.	0.8	1.4	-	V/ns
t <sub>g</sub>	Clock Jitter	CLKA Peak-Peak Period Jitter	-	100	-	ps
t <sub>10</sub>	PLL Lock Time		-	-	3	ms

Figure 2. Test and Measurement Setup



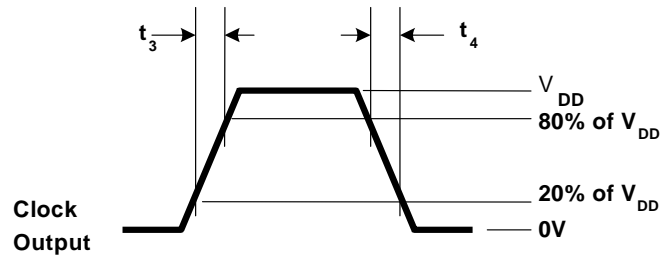
### Voltage and Timing Definitions

Figure 3. Duty Cycle Definitions



Note  
1. Not 100% tested.

Figure 4.  $ER = (0.6 \times V_{DD}) / t_3$ ,  $EF = (0.6 \times V_{DD}) / t_4$



### Ordering Information

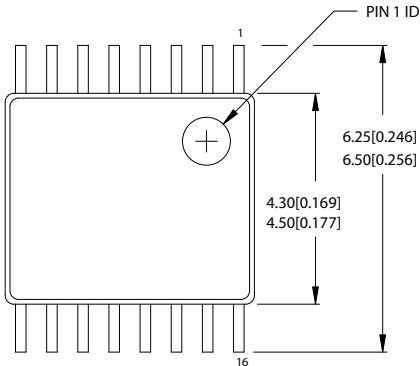
Ordering Code	Package Type	Operating Range	Operating Voltage
<b>Pb-free</b>			
CY24130ZXC-1 <sup>[2]</sup>	16-Pin TSSOP	Commercial	3.3V
CY24130ZXC-1T <sup>[2]</sup>	16-Pin TSSOP – Tape and Reel	Commercial	3.3V
CY24130ZXC-2 <sup>[2]</sup>	16-Pin TSSOP	Commercial	3.3V
CY24130ZXC-2T <sup>[2]</sup>	16-Pin TSSOP – Tape and Reel	Commercial	3.3V
CY24130KZXC-1	16-Pin TSSOP	Commercial	3.3V
CY24130KZXC-1T	16-Pin TSSOP – Tape and Reel	Commercial	3.3V

**Note**

2. Not recommended for new design.

Package Drawing and Dimensions

Figure 5. 16-lead TSSOP 4.40 MM Body Z16.173

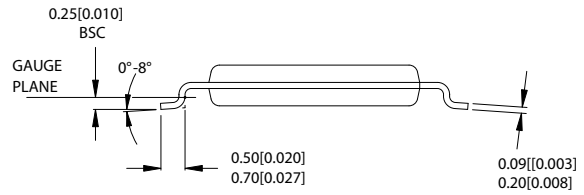
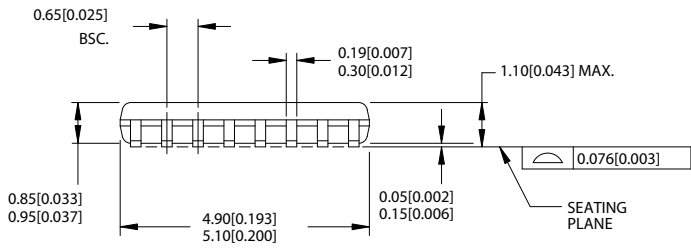


DIMENSIONS IN MM [INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05 gms

PART #	
Z16.173	STANDARD PKG.
ZZ16.173	LEAD FREE PKG.



51-85091-A

## Document History Page

Document Title: CY24130 HOTLink II™ SMPTE Receiver Training Clock				
Document Number: 38-07711				
REV.	ECN NO.	Orig. of Change	Submission Date	Description of Change
**	314514	RGL	See ECN	New Data Sheet
*A	2442066	AESA	See ECN	Updated template. Added Note "Not recommended for new designs." Added part number CY24130KZXC-1, and CY24130KZXC-1T in ordering information table.

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USB	<a href="http://psoc.cypress.com/usb">psoc.cypress.com/usb</a>

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