# PE461X0 Evaluation Kit (EVK) User's Manual

*Monolithic Phase & Amplitude Controller*

## Copyright and Trademarks



## Disclaimers

The information in this document is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

## Patent Statement

Peregrine products are protected under one or more of the following U.S. patents: patents.psemi.com

## Sales Contact

For additional information, contact Sales at sales@psemi.com.

## Corporate Headquarters

9369 Carroll Park Drive, San Diego, CA, 92121

858-731-9400

# Table of Contents

# Introduction

1

## Introduction

The PE461X0 is a HaRP™ technology-enhanced monolithic phase and amplitude controller (MPAC) designed for precise phase and amplitude control of two independent RF paths. It optimizes system performance while reducing manufacturing costs of transmitters that use symmetric or asymmetric power amplifier designs to efficiently process signals with large peak-to-average ratios.

This monolithic RFIC integrates a 90° RF splitter, digital phase shifters and a digital step attenuator along with a low voltage CMOS serial interface. It can cover a phase range of 87.2° in 2.8° steps and an attenuation range of 7.5 dB in 0.5 dB steps, while providing excellent phase and amplitude accuracy from 1.8–2.2 GHz (PE46120), 2.3–2.7 GHz (PE46130) and 3.4–3.8 GHz (PE46140).

The PE461X0 also features exceptional linearity, high output port-to-port isolation and extremely low power consumption relative to competing module solutions. It is offered in a 32-lead 6 × 6 mm QFN package.

The PE461X0 evaluation kit (EVK) includes hardware required to control and evaluate the functionality of the MPAC. The MPAC evaluation software can be downloaded at www.psemi.com and requires a PC running Windows® operating system to control the USB interface board.

### Application Support

For any technical inquiries regarding the evaluation kit or software, please visit applications support at www.psemi.com (fastest response) or call (858) 731-9400.

### Evaluation Kit Contents and Requirements

#### *Kit Contents*

The PE461X0 EVK includes the following hardware required to evaluate the MPAC.

**Table 1 • *PE461X0 Evaluation Kit Contents***

| Quantity | Description |
|---|---|
| 1 | PE461X0 MPAC evaluation board assembly (PRT-55151) |
| 1 | Peregrine USB interface board assembly (PRT-50866) |
| 1 | USB 2.0 Type A to Type B mini cable |

### *Software Requirements*

The MPAC evaluation software will need to be installed on a computer with the following minimum requirements:

- PC compatible with Windows XP, Vista, 7, 8 or 10
- Mouse or other pointing device
- USB port
- HTML browser with internet access
- Administrative privileges

### *Hardware Requirements*

In order to evaluate the performance of the evaluation board, a Vector network analyzer is required.

***Caution:*** The PE461X0 MPAC EVK contains components that might be damaged by exposure to voltages in excess of the specified voltage, including voltages produced by electrostatic discharges. Handle the board in accordance with procedures for handling static-sensitive components. Avoid applying excessive voltages to the power supply terminals or signal inputs or outputs.

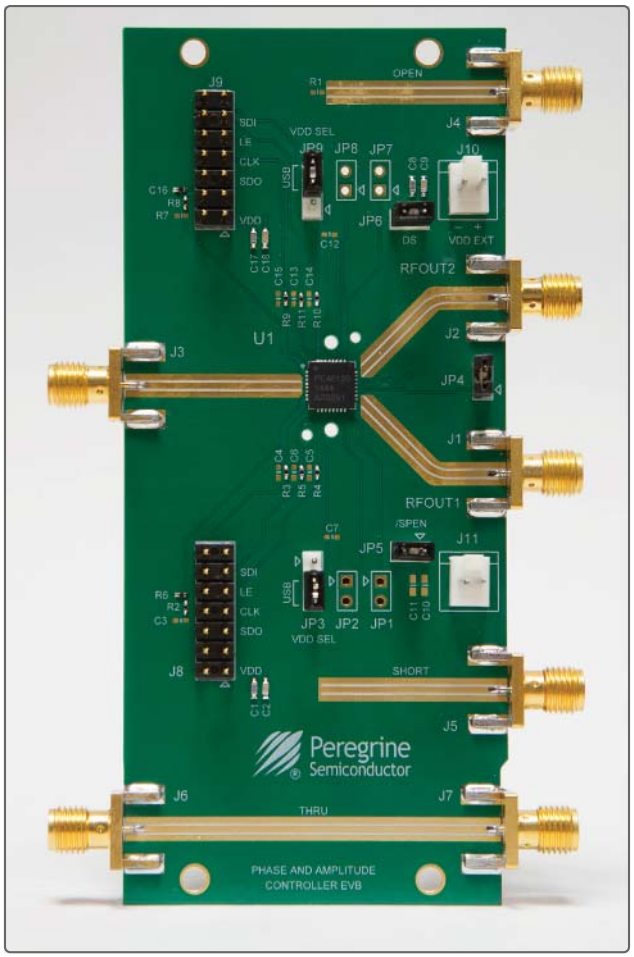
# Evaluation Board Assembly

2

## Evaluation Board Assembly Overview

The evaluation board (EVB) is assembled with a PE461X0, several headers and SMA connectors, as shown in **Figure 1**.

**Figure 1** • ***PE461X0 Evaluation Board Assembly***



This page intentionally left blank.

# Quick Start Guide

3

## Quick Start Overview

The EVB was designed to ease customer evaluation of the PE461X0 MPAC. This chapter will guide the user through the software installation, hardware configuration and using the graphical user interface (GUI).

## Software Installation

### USB Driver

The latest USB interface board drivers are available via Microsoft Windows update. Internet connectivity is required to download the drivers. Connect the USB interface board to the PC and select the Windows Update option to obtain and install the drivers (**Figure 2**).

If the USB board drivers are not installed, it will not be possible to complete the installation of the MPAC EVK software. A USB interface board (**Figure 11**) is included in the evaluation kit.

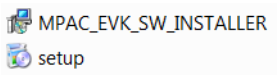
**Figure 2 • *USB Driver Installation (Detecting)***


### EVK Software

In order to evaluate the PE461X0 performance, the application software has to be installed on your computer. The USB interface and MPAC application software is compatible with computers running Windows® XP, Vista, 7, 8 and 10 in 32- or 64-bit configurations. This software is available directly from Peregrine's website at www.psemi.com.

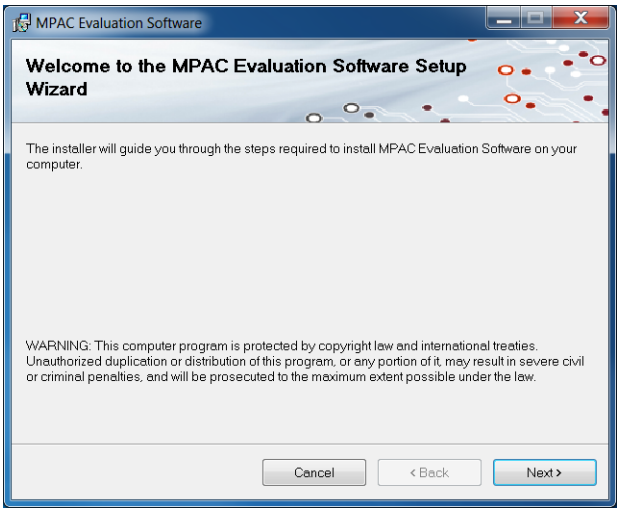
To install the MPAC evaluation software, unzip the archive and execute the "setup.exe" (**Figure 3**).

**Figure 3 • *MPAC Evaluation Software Installer***



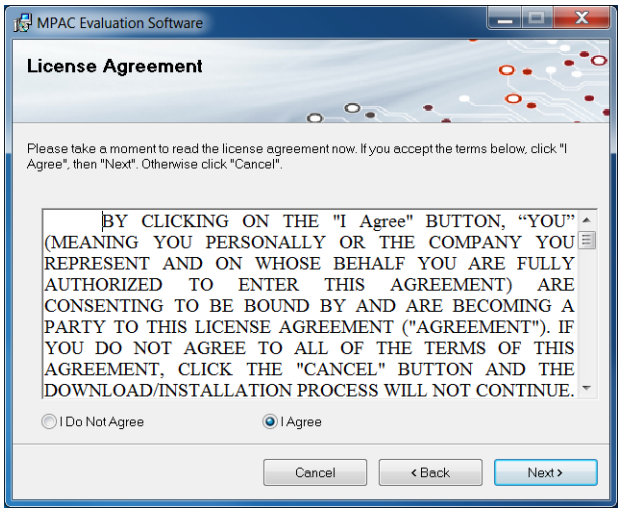

After the setup.exe file has been executed, a welcome screen will appear. It is strongly recommended that all programs be closed prior to running the install program. Click the "Next>" button to proceed.

**Figure 4 • *MPAC Evaluation Software Setup***



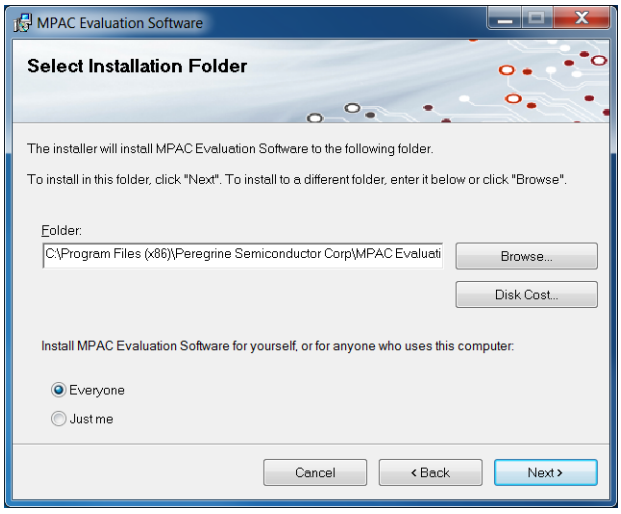
Take a moment to read the license agreement, then click "I Agree" and "Next>."

**Figure 5 • *License Agreement***



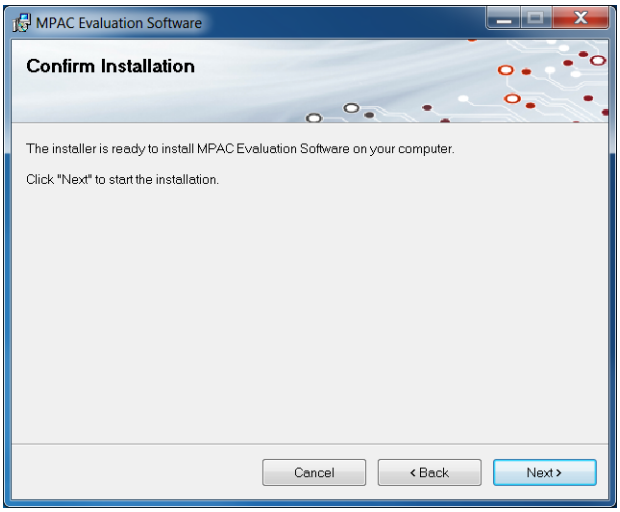

For most users the default install location for the program files is sufficient. If a different location is desired, the install program can be directed to place the program files in an alternate location. The software is installed for "Everyone" by default. Once the desired location is selected click "Next>."

**Figure 6 • *Select Installer Folder***



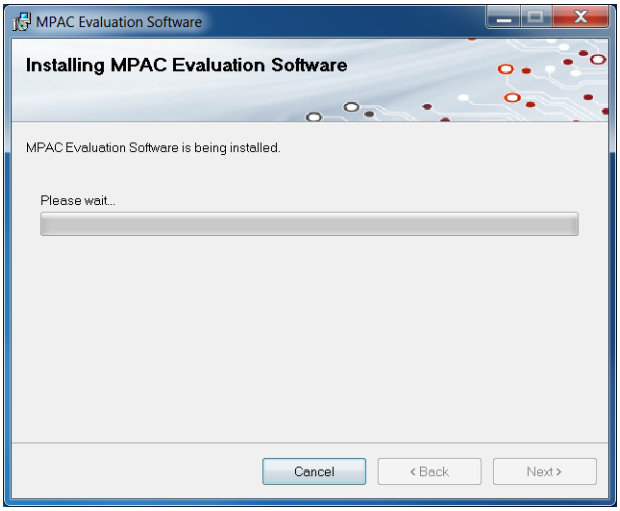

In the window of Confirm Installation, click "Next>" to proceed with the software installation.

**Figure 7 • *Confirm Installation***



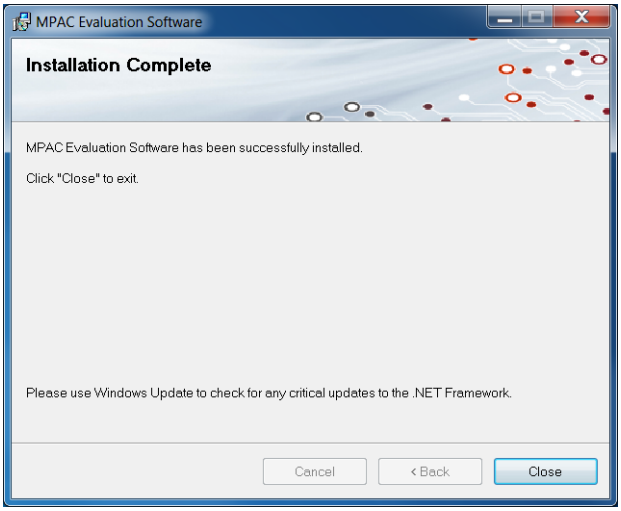

As the software files are installed, a progress indicator will be displayed. On slower computers, installation of the software may proceed for a few moments.

**Figure 8 • *Progress Indicator***



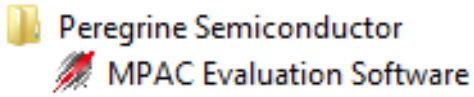
Once the evaluation software is installed, click "Close" to exit.

**Figure 9 • *Installation Complete***




A new Start Menu item under Peregrine Semiconductor will appear in the start menu of your computer. Select "MPAC Evaluation Software" to launch the GUI.

**Figure 10 • *MPAC Evaluation Software Launch***

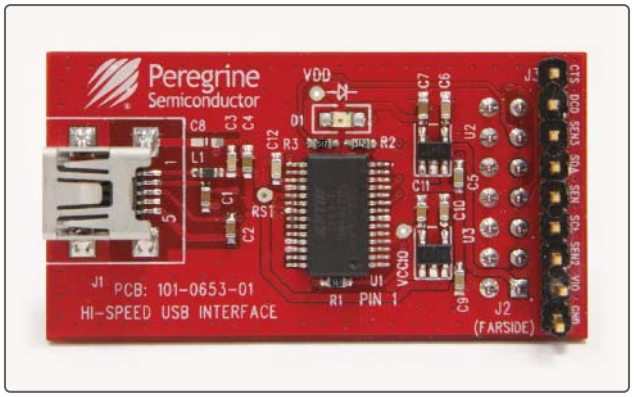


# Hardware Configuration

## USB Interface Board Overview

The USB interface board (**Figure 11**) is included in the evaluation kit. This board allows the user to send serial peripheral interface (SPI) commands to the device under test by using a PC running the Windows operating system. To install the software, refer to "**Software Installation**".

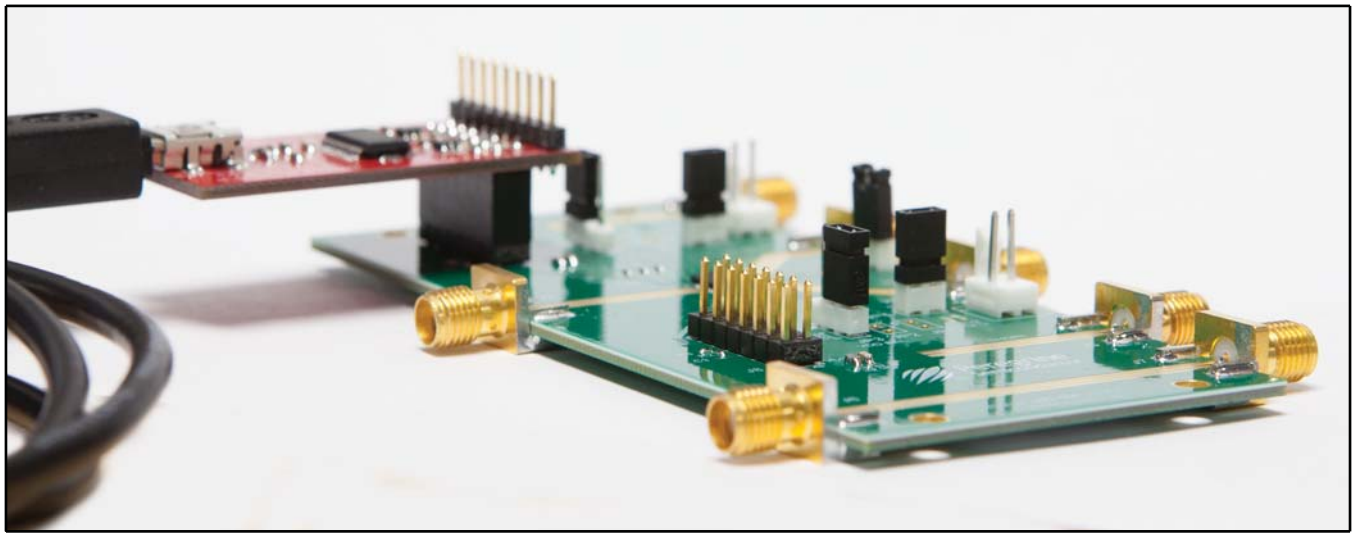
**Figure 11** • *USB Interface Board*




## Connection of the USB Interface Board to the Evaluation Board

The EVB and the USB interface board contain a 14-pin header. This feature allows the USB interface board (socket) to connect directly to the EVB (pin) on the front side as shown in **Figure 12**. Use caution when making the connection to ensure the USB interface board is aligned and connected to both rows of pins properly.

**Figure 12** • *USB Interface Board Connected to the Evaluation Board*



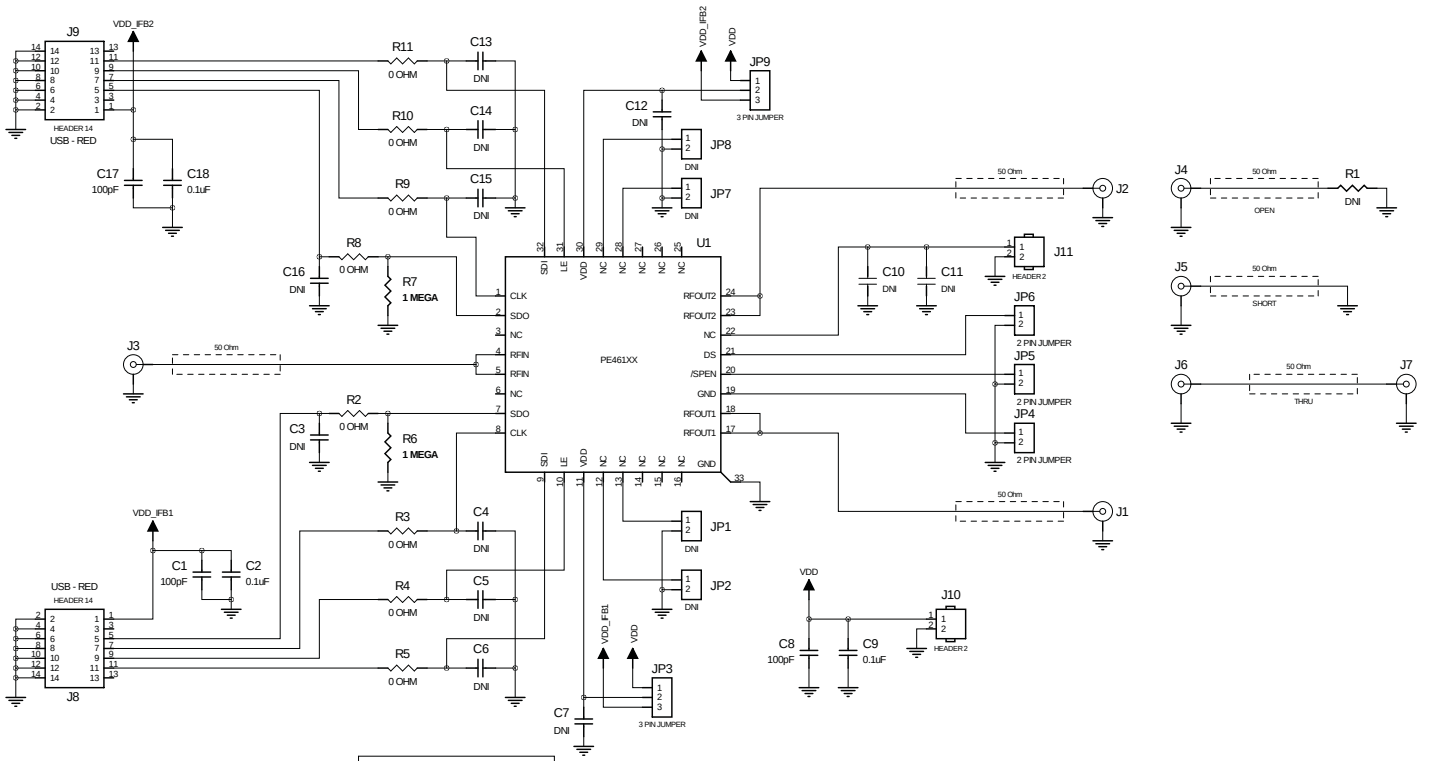
## Evaluation Board Overview

The evaluation board is designed to ease customer evaluation of Peregrine's products. The board contains:

1) Standard 0.1 inch headers are provided for power supply, digital control signals and USB interface board.
2) SMA connectors are provided for RF performance verification and connecting the THRU trace to calibrate board trace loss.

The schematic and evaluation board outline are provided in this user manual.

**Figure 13 • *PE461X0 Evaluation Board Schematic***

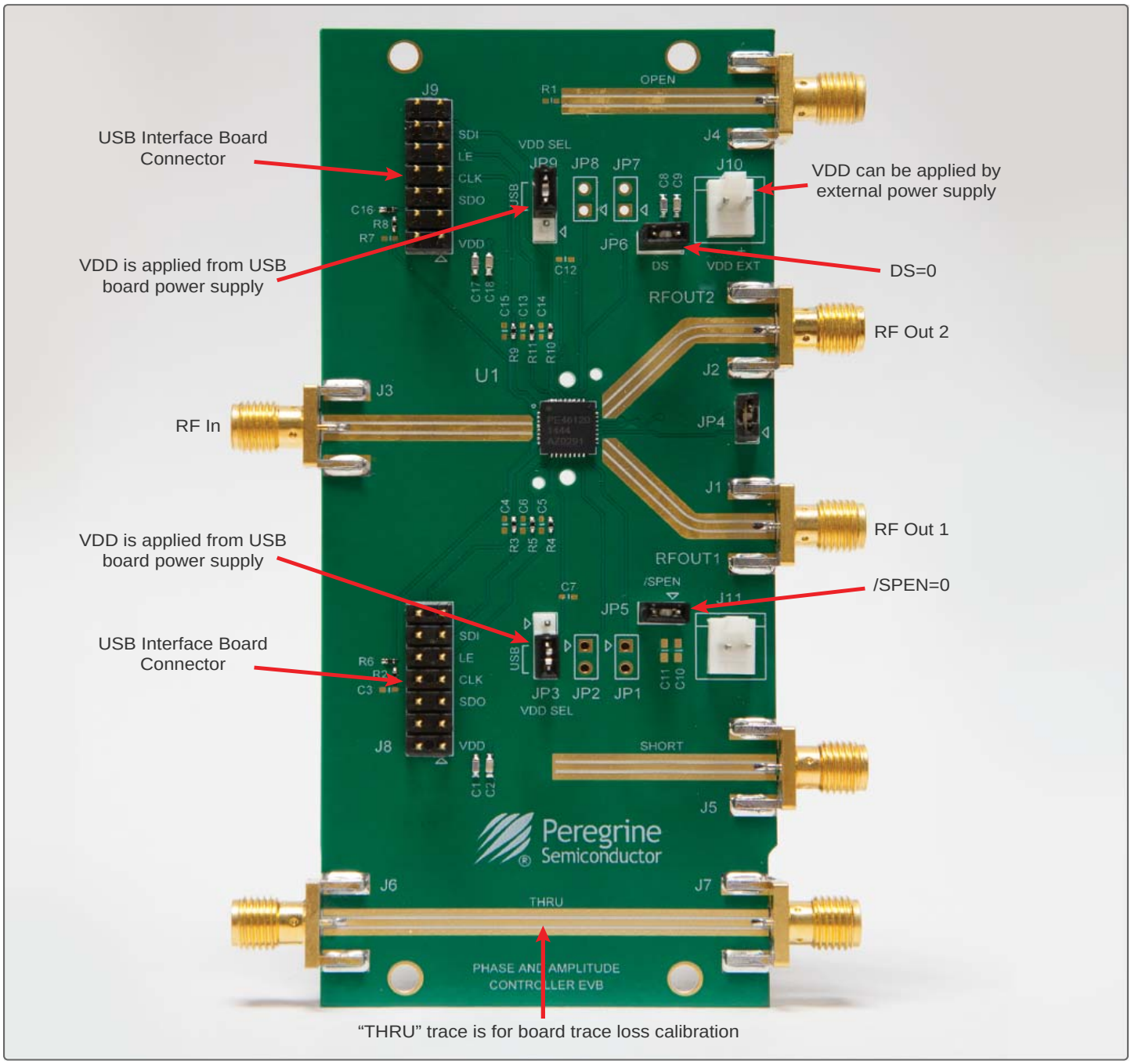



| INSTALL LOGIC JUMPERS ON | |
|---|---|
| REF DES | PINS |
| JP3 | 2-3 |
| JP4 | 1-2 |
| JP5 | 1-2 |
| JP6 | 1-2 |
| JP9 | 2-3 |

*NOTES:*

*1. CAUTION:*
*CONTAINS PARTS AND ASSEMBLIES SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGE (ESD)*

**Figure 14 •** ***PE461X0 Evaluation Board Outline Showing Functional Overview***



## Hardware Operation

The general guidelines for operating the hardware evaluation board are listed in this section. Follow the steps below to configure the hardware for basic evaluation.

1) Install the jumper on JP4, JP5 and JP6.
   a) JP4 connects to PE461X0 pin 19 (GND) to ground.
   b) JP5 connects to PE461X0 pin 20 (/SPEN) to ground for normal SPI operation.
   c) JP6 connects to PE461X0 pin 21 (DS) to ground as DS = 0 setting.
2) There are two options to provide PE461X0 a power supply. They are:
   a) Option 1: Power up through USB interface board. The evaluation board is configured for this option by installing a jumper on JP3 pin 2–3 and a jumper on JP9 pin 2–3 (refer to **Figure 14**).
   b) Option 2: Power via external power supply. The evaluation board is configured for this option by installing a jumper on JP3 pins 1–2 and a jumper on JP9 pins 1–2 (refer to **Figure 14**). Connect the external power supply to $V_{DD\_EXT}$ J10 or J11 (pin 1+, pin 2–).
3) Plug in USB interface board on J8 or J9, as shown in **Figure 11**. J8 and J9 provide identical control to the device.
4) Calibrate board trace loss and phase with THRU trace between J6 and J7. THRU calibration is sufficient for initial measurements. If more accurate results are desired, the full set of SOLT standards can be used.

**Table 2 • *Recommended Operating Condition for PE461X0***

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Supply voltage, $V_{DD}$ (1) | 2.3 | | 5.5 | V |
| Supply current | | 350 | 500 | µA |
| Digital input high | 1.17 | | 3.6 | V |
| Digital input low | 0 | | 0.6 | V |
| Digital input leakage | | 10 | 20 | µA |
| RF input power, CW | | | 29 | dBm |
| RF input power, pulsed (2) | | | 32 | dBm |
| Operating temperature range | –40 | +25 | +105 | °C |

**Notes:**
1) Product performance does not vary over $V_{DD}$.
2) Pulsed, 5% duty cycle of 4620 µs period.

**Table 3 • *Bit Descriptions***

| | |
|---|---|
| C0 | Channel register select |
| | C0 = L, channel $RF_{OUT1}$ register select |
| | C0 = H, channel $RF_{OUT2}$ register select |
| M0–M3 | Attenuation setting |
| P0–P4 | Phase shift setting per channel |
| S0–S3 | Spare bits (PE46120)<br>Insertion loss stabilizer (ILS) setting per channel (PE46130/PE46140) |

**Table 4 • *14-bit Word (PE46120)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 |
| 1 | — | — | — | — | — | — | 45° | 22.5° | 11.2° | 5.6° | 2.8° | — | — |
| 2 | — | — | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | — | — |

**Table 5 • *Serial Truth Table—Phase Setting (PE46120)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Phase Shift Setting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| 1/2 | — | — | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | — | — | |
| X | X | X | X | X | X | X | L | L | L | L | L | X | X | Ref phase |
| X | X | X | X | X | X | X | L | L | L | L | H | X | X | 2.8 deg |
| X | X | X | X | X | X | X | L | L | L | H | L | X | X | 5.6 deg |
| X | X | X | X | X | X | X | L | L | H | L | L | X | X | 11.25 deg |
| X | X | X | X | X | X | X | L | H | L | L | L | X | X | 22.5 deg |
| X | X | X | X | X | X | X | H | L | L | L | L | X | X | 45 deg |
| X | X | X | X | X | X | X | H | H | H | H | H | X | X | 87.2 deg |

**Table 6 • *14 Bit Word (PE46130)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 |
| 1 | — | — | — | — | — | — | 45° | 22.5° | 11.2° | 5.6° | 2.8° | — | — |
| 2 | — | 0.2 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.1 | 0.05 |

**Table 7 • *Serial Truth Table—Phase Setting (PE46130)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Phase Shift Setting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| 1/2 | — | 0.2 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.1 | 0.05 | |
| X | L | X | X | X | X | X | L | L | L | L | L | X | X | Ref phase |
| X | L | X | X | X | X | X | L | L | L | L | H | X | X | 2.8 deg |
| X | L | X | X | X | X | X | L | L | L | H | L | X | X | 5.6 deg |
| X | L | X | X | X | X | X | L | L | H | L | L | X | X | 11.25 deg |
| X | L | X | X | X | X | X | L | H | L | L | L | X | X | 22.5 deg |
| X | L | X | X | X | X | X | H | L | L | L | L | X | X | 45 deg |
| X | L | X | X | X | X | X | H | H | H | H | H | X | X | 87.2 deg |

**Table 8 • *14-bit Word (PE46140)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 |
| 1 | — | — | — | — | — | — | 45° | 22.5° | 11.2° | 5.6° | 2.8° | — | — |
| 2 | — | 0.25 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.125 | 0.0625 |

**Table 9 • *Serial Truth Table—Phase Setting (PE46140)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Phase Shift Setting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| 1/2 | — | 0.25 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.125 | 0.0625 | |
| X | L | X | X | X | X | X | L | L | L | L | L | X | X | Ref phase |
| X | L | X | X | X | X | X | L | L | L | L | H | X | X | 2.8 deg |
| X | L | X | X | X | X | X | L | L | L | H | L | X | X | 5.6 deg |
| X | L | X | X | X | X | X | L | L | H | L | L | X | X | 11.25 deg |
| X | L | X | X | X | X | X | L | H | L | L | L | X | X | 22.5 deg |
| X | L | X | X | X | X | X | H | L | L | L | L | X | X | 45 deg |
| X | L | X | X | X | X | X | H | H | H | H | H | X | X | 87.2 deg |

**Table 10 • *Serial Truth Table—Attenuation Setting $RF_{OUT2}$ (PE46120)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Amplitude Setting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| 2 | — | — | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | — | — | |
| H | X | X | L | L | L | L | X | X | X | X | X | X | X | Ref insertion loss |
| H | X | X | L | L | L | H | X | X | X | X | X | X | X | 0.5 dB |
| H | X | X | L | L | H | L | X | X | X | X | X | X | X | 1 dB |
| H | X | X | L | H | L | L | X | X | X | X | X | X | X | 2 dB |
| H | X | X | H | L | L | L | X | X | X | X | X | X | X | 4 dB |
| H | X | X | H | H | H | H | X | X | X | X | X | X | X | 7.5 dB |

**Table 11 • *Default State Settings at Power Up $RF_{OUT1}$ (PE46120)***

| DS Setting | Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Default Setting at Power Up |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| | 1/2 | — | — | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | — | — | |
| DS = 0 | — | — | — | — | — | — | — | L | L | L | L | L | — | — | 0 dB<br>0 deg |
| DS = 1 | — | — | — | — | — | — | — | H | L | L | L | L | — | — | 0 dB<br>45 deg |

**Table 12 • *Default State Setting at Power Up $RF_{OUT2}$ (PE46120)***

| DS Setting | Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q4 | Q3 | Q2 | Q1 | Default Setting at Power Up |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| | 1/2 | — | — | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | — | — | |
| DS = 0 | — | — | — | L | L | L | L | L | L | L | L | L | — | — | 0 dB<br>0 deg |
| DS = 1 | — | — | — | H | H | H | H | H | L | L | L | L | — | — | 7.5 dB<br>45 deg |

**Table 13 • *Serial Truth Table—Attenuation Setting $RF_{OUT2}$ (PE46130)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Amplitude Setting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| 2 | — | 0.2 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.1 | 0.05 | |
| H | L | X | L | L | L | L | X | X | X | X | X | X | X | Ref insertion loss |
| H | L | X | L | L | L | H | X | X | X | X | X | X | X | 0.5 dB |
| H | L | X | L | L | H | L | X | X | X | X | X | X | X | 1 dB |
| H | L | X | L | H | L | L | X | X | X | X | X | X | X | 2 dB |
| H | L | X | H | L | L | L | X | X | X | X | X | X | X | 4 dB |
| H | L | X | H | H | H | H | X | X | X | X | X | X | X | 7.5 dB |

**Table 14 • *Default State Settings at Power Up $RF_{OUT1}$ (PE46130)***

| DS Setting | Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Default Setting at Power Up |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| | 1/2 | — | 0.2 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.1 | 0.05 | |
| DS = 0 | — | — | — | — | — | — | — | L | L | L | L | L | — | — | 0 dB<br>0 deg |
| DS = 1 | — | — | — | — | — | — | — | H | L | L | L | L | — | — | 0 dB<br>45 deg |

**Table 15 • *Default State Settings at Power Up $RF_{OUT2}$ (PE46130)***

| DS Setting | Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Default Setting at Power Up |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| | 1/2 | — | 0.2 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.1 | 0.05 | |
| DS = 0 | — | L | L | L | L | L | L | L | L | L | L | L | L | L | 0 dB<br>0 deg |
| DS = 1 | — | L | L | H | H | H | H | H | L | L | L | L | L | L | 7.5 dB<br>45 deg |

**Table 16 • *Serial Truth Table—Attenuation Setting $RF_{OUT2}$ (PE46140)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Amplitude Setting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| 2 | — | 0.25 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.125 | 0.0625 | |
| H | L | X | L | L | L | L | X | X | X | X | X | X | X | Ref insertion loss |
| H | L | X | L | L | L | H | X | X | X | X | X | X | X | 0.5 dB |
| H | L | X | L | L | H | L | X | X | X | X | X | X | X | 1 dB |
| H | L | X | L | H | L | L | X | X | X | X | X | X | X | 2 dB |
| H | L | X | H | L | L | L | X | X | X | X | X | X | X | 4 dB |
| H | L | X | H | H | H | H | X | X | X | X | X | X | X | 7.5 dB |

**Table 17 • *Default State Settings at Power Up $RF_{OUT1}$ (PE46140)***

| DS Setting | Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Default Setting at Power Up |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| | 1/2 | — | 0.25 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.125 | 0.0625 | |
| DS = 0 | — | — | — | — | — | — | — | L | L | L | L | L | — | — | 0 dB<br>0 deg |
| DS = 1 | — | — | — | — | — | — | — | H | L | L | L | L | — | — | 0 dB<br>45 deg |

**Table 18 • *Default State Settings at Power Up $RF_{OUT2}$ (PE46140)***

| DS Setting | Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Default Setting at Power Up |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| | 1/2 | — | 0.25 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.125 | 0.0625 | |
| DS = 0 | — | L | L | L | L | L | L | L | L | L | L | L | L | L | 0 dB<br>0 deg |
| DS = 1 | — | L | L | H | H | H | H | H | L | L | L | L | L | L | 7.5 dB<br>45 deg |

## Insertion Loss Stabilizer

The PE46130/PE46140 offer greater insertion loss stability (ILS) by compensating for known variations between phase states. Three attenuation bits are used to reduce the variation seen in the insertion loss across all phase states for the $RF_{OUT2}$ path. ILS bits S0–S2 are accessible for creating a custom lookup table in applications where insertion loss variation between phase states is critical. PE46120 does not support this feature.

**Table 19 • *Insertion Loss Stabilizer Bit Definition (PE46130)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Amplitude Setting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| 2 | — | 0.2 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.1 | 0.05 | |
| H | L | L | X | X | X | X | X | X | X | X | X | L | L | Ref IL |
| H | L | L | X | X | X | X | X | X | X | X | X | L | H | 0.05 dB |
| H | L | L | X | X | X | X | X | X | X | X | X | H | L | 0.1 dB |
| H | L | H | X | X | X | X | X | X | X | X | X | L | L | 0.2 dB |
| H | L | H | X | X | X | X | X | X | X | X | X | H | H | 0.35 dB |

**Table 20 • *Insertion Loss Stabilizer Bit Definition (PE46140)***

| Q13 | Q12 | Q11 | Q10 | Q9 | Q8 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Amplitude Setting |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C0 | S3 | S2 | M3 | M2 | M1 | M0 | P4 | P3 | P2 | P1 | P0 | S1 | S0 | |
| 1/2 | — | 0.25 | 4 | 2 | 1 | 0.5 | 45° | 22.5° | 11.2° | 5.6° | 2.8° | 0.125 | 0.0625 | |
| H | L | L | X | X | X | X | X | X | X | X | X | L | L | Ref IL |
| H | L | L | X | X | X | X | X | X | X | X | X | L | H | 0.0625 dB |
| H | L | L | X | X | X | X | X | X | X | X | X | H | L | 0.125 dB |
| H | L | H | X | X | X | X | X | X | X | X | X | L | L | 0.25 dB |
| H | L | H | X | X | X | X | X | X | X | X | X | H | H | 0.4375 dB |

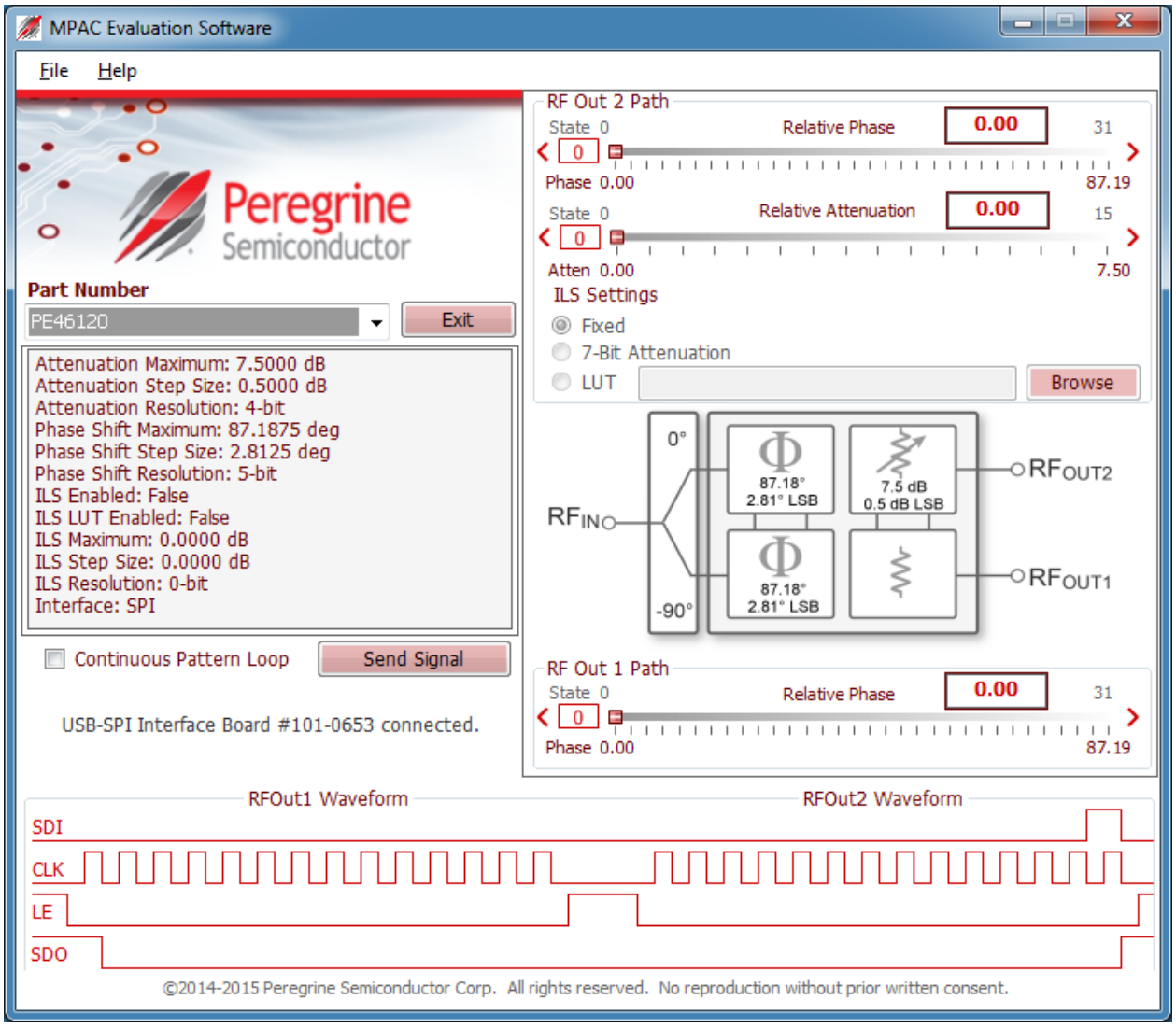
# Using the Graphical User Interface

**Figure 15** displays the MPAC application software graphical user interface (GUI), which has the USB interface board plugged into the computer. The message "USB-SPI Interface Board #101-0653 connected" will indicate that the USB interface board is connected and recognized. See "**Hardware Operation**" on page 11 for detailed information regarding hardware configuration for use with the GUI control software. If the USB interface board is not connected when the application software is launched, the message "No interface board connected! Please connect USB-SPI Interface #101-0653" will appear at the bottom of the screen.

In the upper left corner, under the Peregrine logo, there is a drop-down menu item to select the part number for evaluation and the part description is below the part number box.

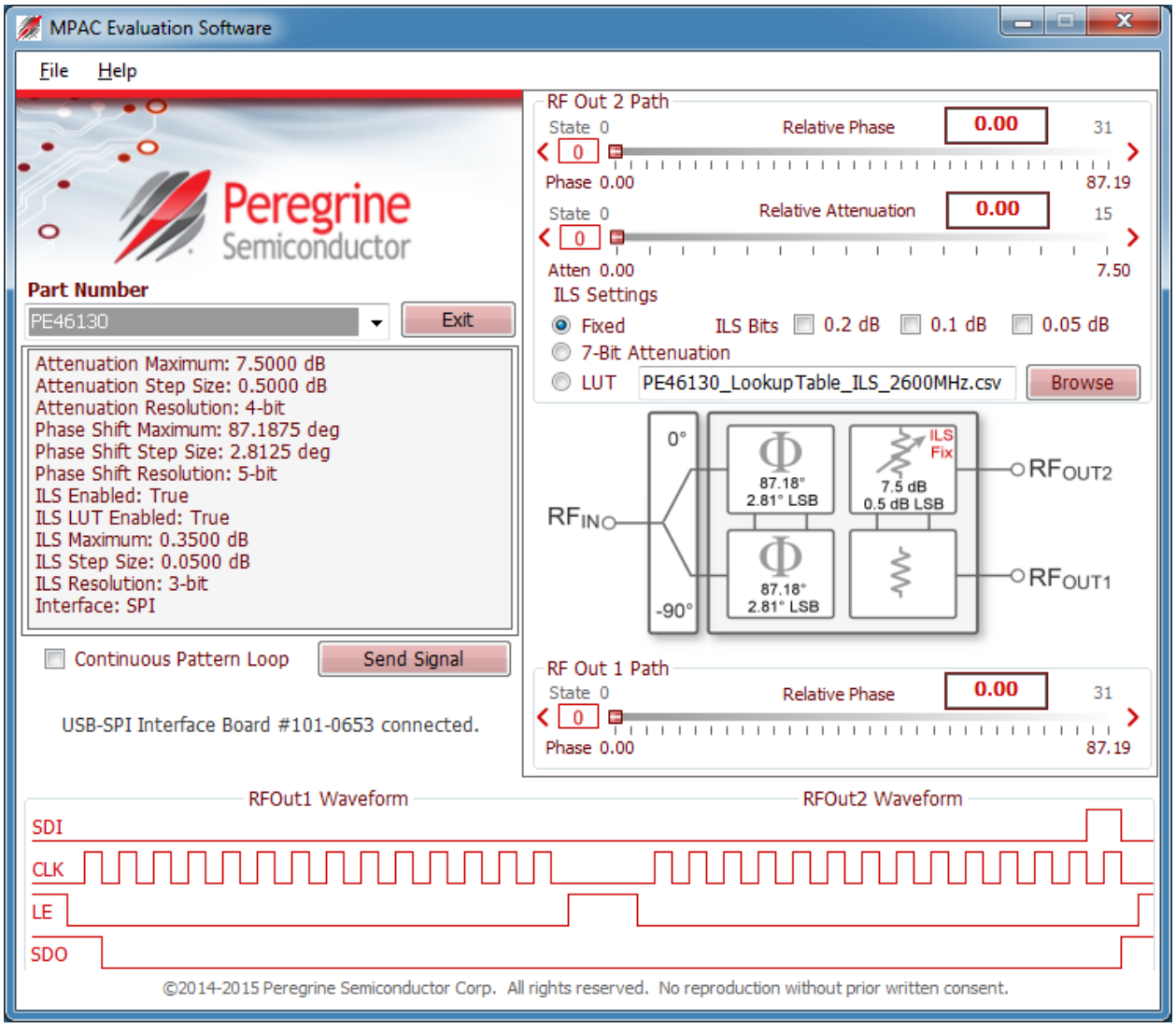
The MPAC application software GUI is displayed in **Figure 15** and illustrates the available controls and messages available to the user.

**Figure 15 •** ***PE46120 Application Software Graphical User Interface***(*)



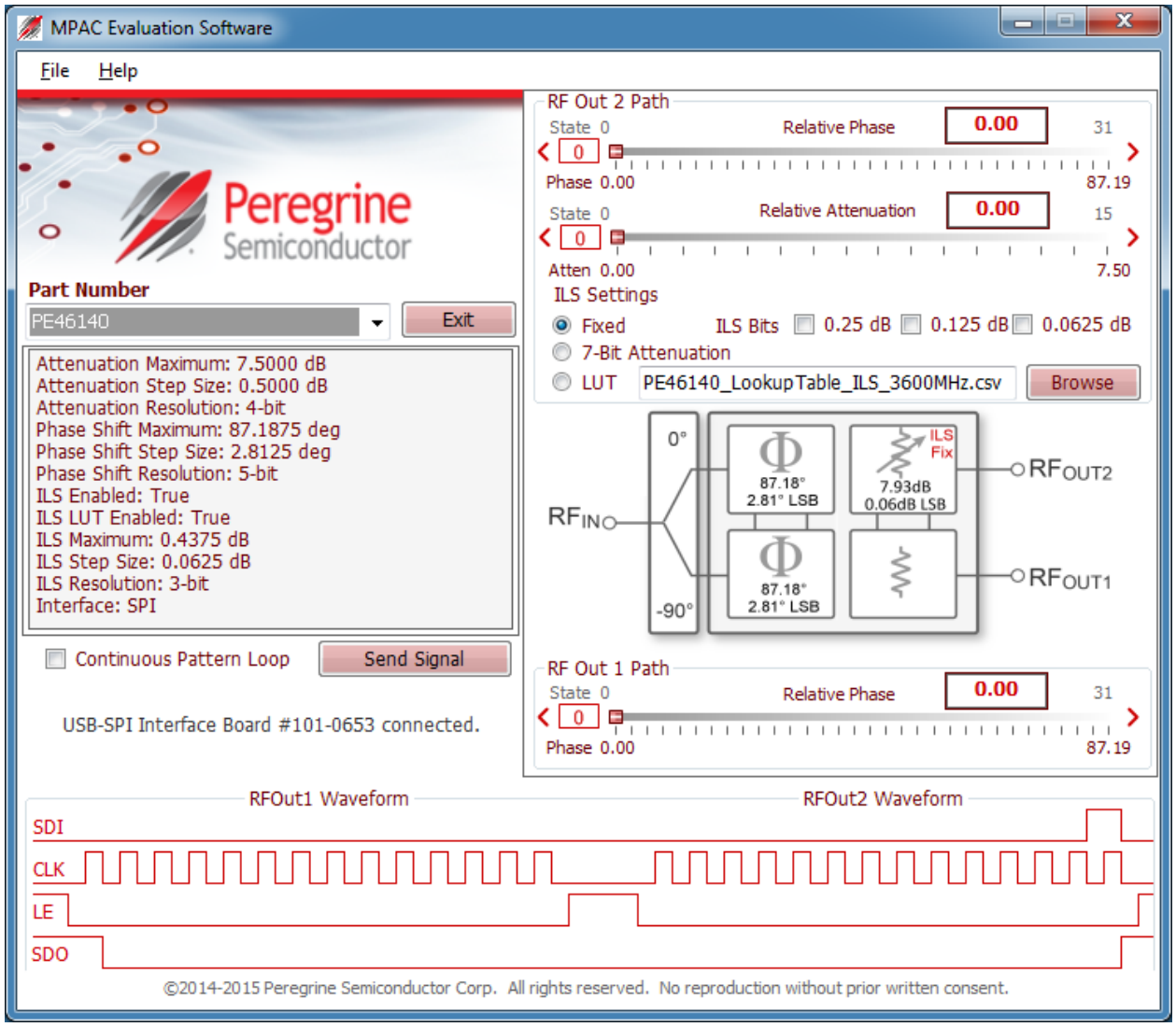

**Note:** * SDO in the serial interface waveform is read back from the MPAC to verify SDO toggling to indicate proper communication with the MPAC.

**Figure 16 • *PE46130 Application Software Graphical User Interface*(*)**




**Note: *** SDO in the serial interface waveform is read back from the MPAC to verify SDO toggling to indicate proper communication with the MPAC.

**Figure 17 • *PE46140 Application Software Graphical User Interface*(*)**

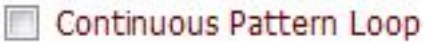



**Note:** * SDO in the serial interface waveform is read back from the MPAC to verify SDO toggling to indicate proper communication with the MPAC.

### *Continuous Pattern Loop*

The continuous pattern loop checkbox (see Figure 18) allows the user to observe the evaluation board automatically step through each of the phase and attenuation states. Once the GUI reaches the maximum state value the cycle begins again at the minimum state value. This function can be started and stopped at any time by selecting/deselecting the checkbox.

**Figure 18 • *Continuous Pattern Loop***




### *Send Signal*

The "Send Signal" box can be used to resend the same data.

**Figure 19 • *Send Signal***

### *Attenuation and Phase Slide Bar*

The RF Out X Path slide bars allow the user to quickly select the desired attenuation and phase. The arrows at the left and right can be clicked to increase or decrease phase or attenuation state at the minimum step size. The attenuation and phase value text box is updated with each change of the phase slider. This control is two-way; the user can also enter a valid attenuation and phase value into this text box followed by the ENTER key to program the hardware with the updated value.

**Figure 20 • *$RF_{OUT1}$ Path Slide Bar***

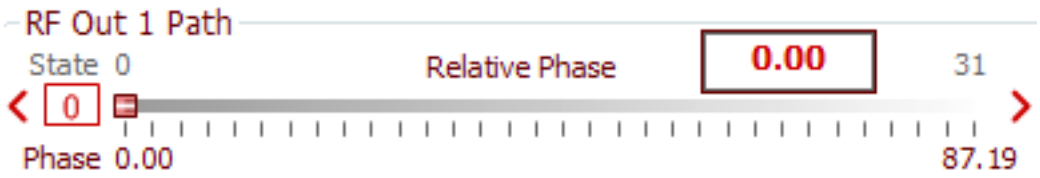
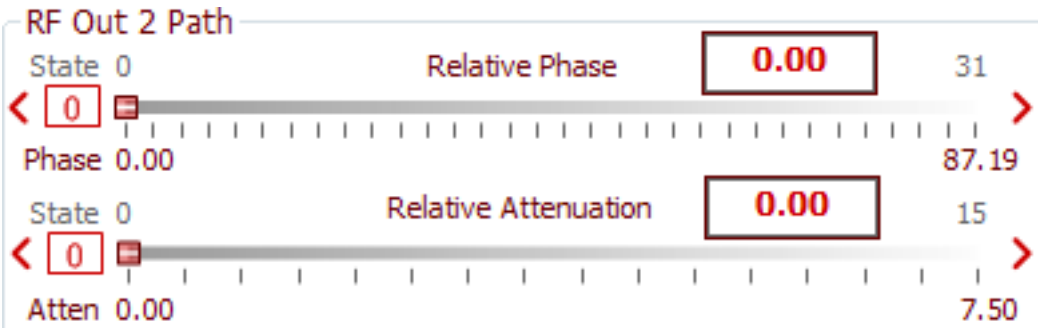



**Figure 21 • *$RF_{OUT2}$ Path Slide Bar***



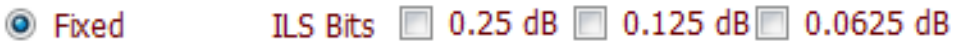
### *ILS Settings*

The available ILS bit options are shown in **Figure 22**–**Figure 24**. PE46120 does not support the ILS feature and the controls are disabled when evaluating this device. In **Figure 22**, fixed ILS bits are selected during the attenuation and value is programmed. In **Figure 23**, three of the ILS bits along with the 4-bit digital step attenuation are programmed for the attenuation value. In **Figure 24**, the lookup table (LUT) is selected for attenuation value programming.

#### Fixed ILS Bits

The MPAC GUI supports manual control of the ILS bits. These bits allow for the user to add small amounts of attenuation to reduce amplitude variations between phase states. These binary attenuation bits are enabled by clicking the square box to enable the additional attenuation.

**Figure 22 • *Fixed ILS Bits***




#### 7-bit Attenuation

The MPAC GUI supports extending the ILS bits to become three additional attenuation control bits in addition to the standard four bits for a total of 7 attenuation bits. This updates the GUI controls (attenuation slider and text box data entry) to achieve finer attenuation steps for applications that require finer attenuation control.

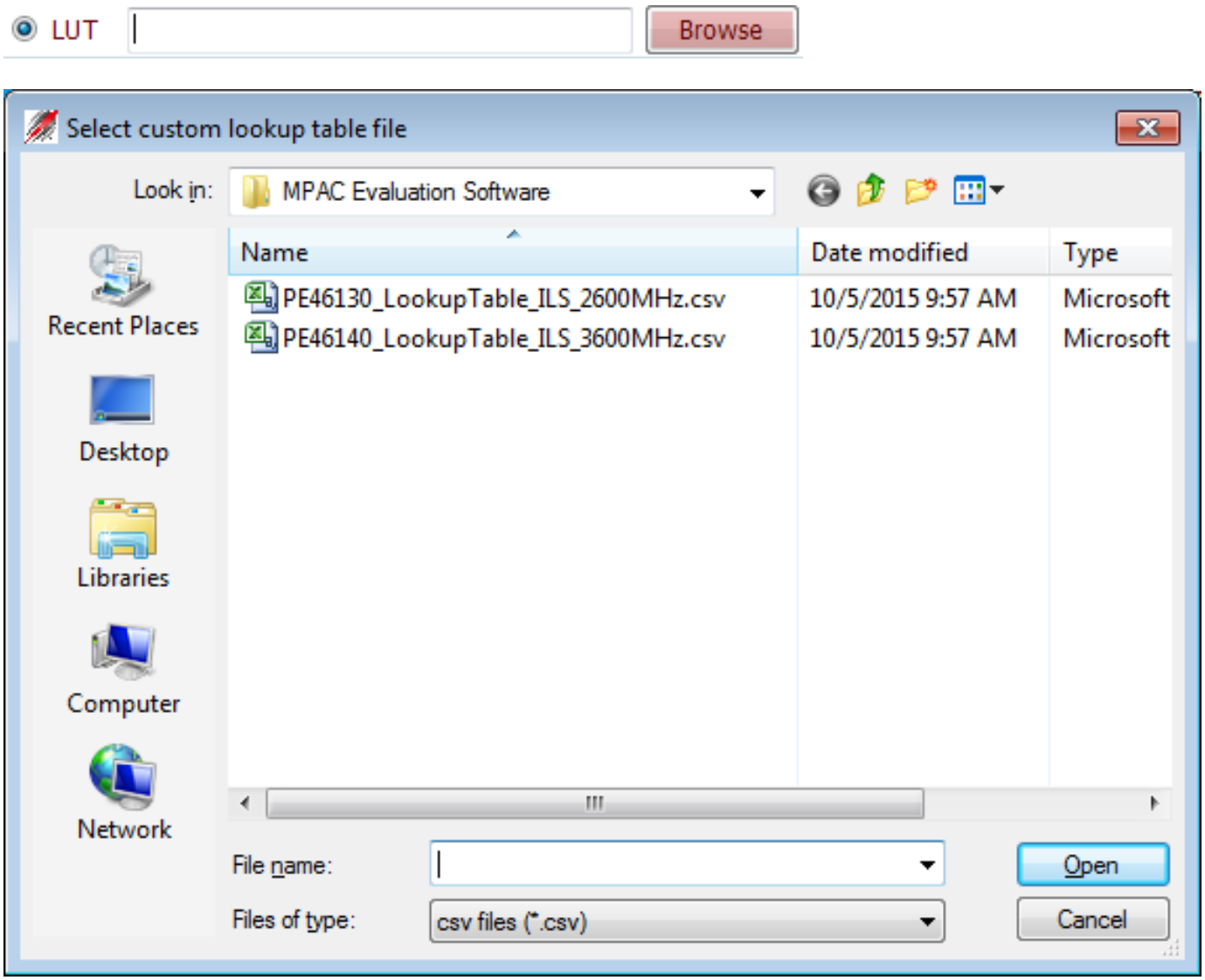
**Figure 23 • *7-bit Attenuation***

Lookup Table Enable and File Selection

The MPAC GUI supports a LUT in a text based .csv file format to demonstrate control of ILS bits S0–S2 for reduced amplitude variations between phase states. Peregrine includes one sample LUT for the PE46130 and PE46140 at the device center frequency. These tables are frequency dependent due to the phase shifter and can be tailored to a specific frequency. A new LUT file can be generated by the user following the data format provided in the header of the sample LUT files. The user may also contact application engineering support for assistance generating custom LUTs at specific frequencies.

Activate the LUT function by selecting the LUT radio button. A file dialog box (**Figure 23**) will require the user to select the LUT that is suitable for the device being evaluated. To change to a different LUT, click the browse button (**Figure 24**) to show the file dialog box (**Figure 23**) and choose the desired LUT for the device being evaluated.

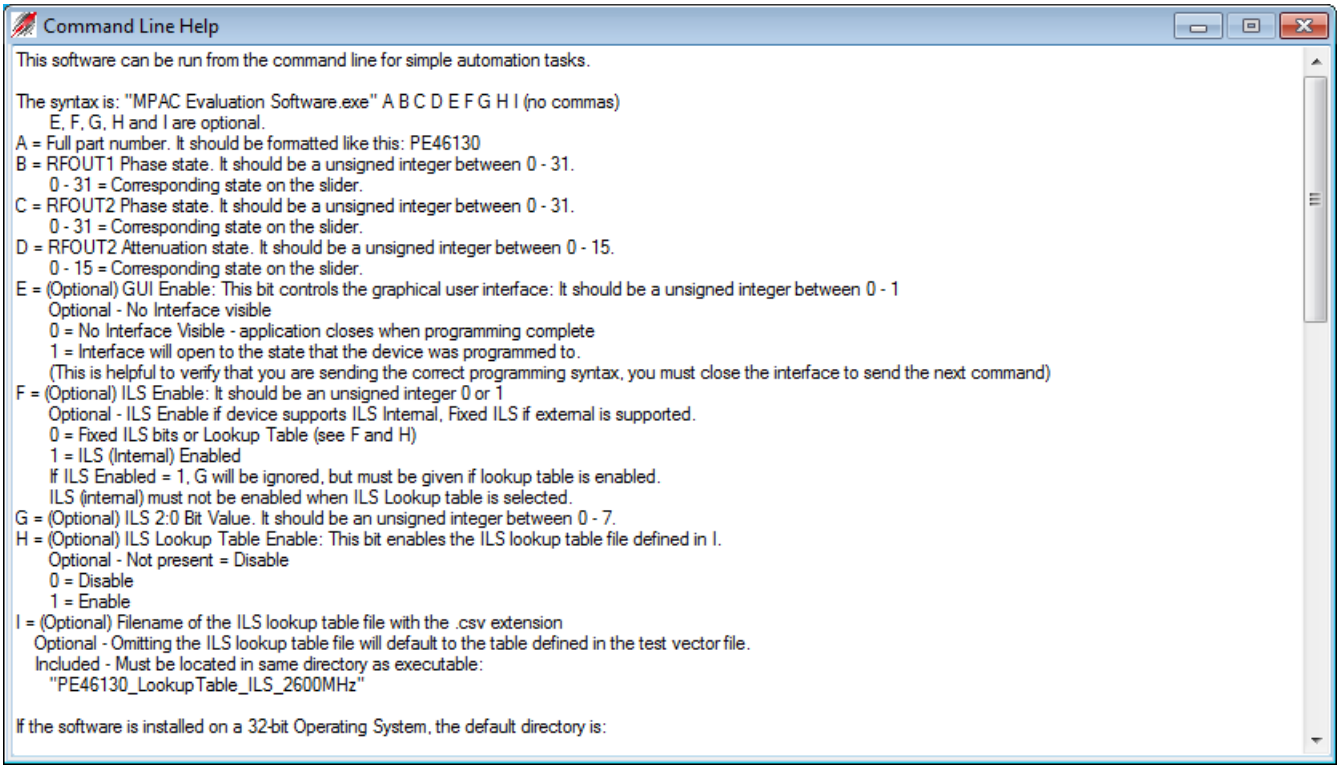
**Figure 24 • *Lookup Table Enable and File Selection***



# Help

The MPAC software contains a help section with information on using the evaluation software via a command line interface to aid in the evaluation of the phase shifter. To access the command line help, click HELP on the menu bar item, then click on COMMAND LINE (see **Figure 25**).

**Figure 25 • *Command Line Control***



# Technical Resources

4

## Technical Resources

Additional technical resources are available for download in the Products section at www.psemi.com. These include the Product Specification datasheet, state dependent S-parameters, zip file, evaluation kit schematic and bill of materials, material declaration form and PC-compatible software file.

Trademarks are subject to trademark claims.

This page intentionally left blank.