DATASHEET

Dual Intermediate Frequency Digital Variable Gain Amplifier

IDTF1240NBGI

General Description

The IDTF1240 (0.5 dB steps) is an IF VGA for Diversity Basestation receivers. The device offers significantly better Noise and Distortion performance than currently available devices. It is packaged in a compact 5x5 Thin QFN with 200 ohm differential input and output impedances for ease of integration into the receiver lineup.

Competitive Advantage

The IDTF1240 IF VGA improves system SNR, especially at lower gain settings. Via IDT's proprietary FlatNoise™ technology both **$IP3_O$ & NF are kept virtually flat** while gain is backed off, enhancing SNR significantly under high level interferer conditions, and greatly benefiting 2G/3G/4G Multi-Carrier IF sampling receivers.

The fast-settling, parallel mode gain step of 0.50 dB coupled with the excellent differential non-linearity allow for SNR to be maximized further by targeting the minimum necessary gain in small, accurate increments.

The matched output does not require a terminating resistor, thus the gain and distortion performance are preserved when driving Bandpass Anti-Alias filters.

See the 'Applications Information' section starting on Page 19 for more details of the benefits of the F1240 in IF sampling receivers.

Part# Matrix

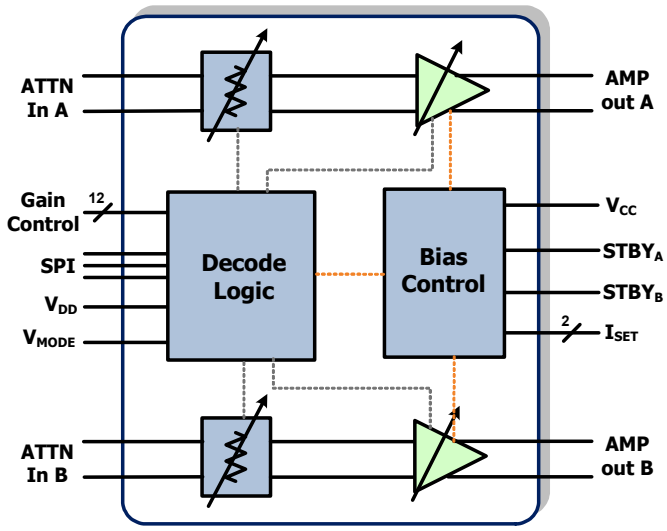
Part#	Range / Step	$IP3_O$	IF freq range	NF	Pinout Compatibility
F1240	**20 to -11.5 0.5**	**47**	**10 - 500**	**4**	**NSM**
F1241	20 to -11 1.0	47	10 - 500	4	ADI

Ordering Information

Features

- Ideal for systems with high SNR requirements
- 20 dB typical Maximum Gain
- 31.5 dB gain control range
- 6 bit control
- 0.50 dB Gain Steps
- **Excellent Noise Figure = 4.0 dB**
- 5mm x 5mm 32 pin package
- **200** Ω Differential Matched Input
- **200** Ω Differential Matched Output
- No termination resistors required
- **NF degrades just 1.3 dB @ 10 dB below Max Gain**
- 10 MHz – 500 MHz frequency range
- Ultra-Linear: **$IP3_O$ +47 dBm** typical
- Excellent 2nd Harmonic Rejection
- Selectable Parallel or Serial Control
- External current setting resistors
- Very fast settling < 15 nsec
- Individual Power Down Modes
- Extremely Low Power: **80 mA / Chan**

Device Block Diagram



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND	-0.3V to +5.5V
GA[5-0], GB[5-0], DATA, CSb, CLK, V_{MODE}, $STBY_A$, $STBY_B$	-0.3V to (VCC_ + 0.25V)
OUT_A-, OUT_A+, OUT_B-, OUT_B+	-0.3V to (VCC_ + 0.25V)
IN_A-, IN_A+, IN_B-, IN_B+	-0.3V to +2.2V
ISET_A, ISET_B to GND	-0.3V to +2.2V
RF Input Power (IN_A-, IN_A+, IN_B-, IN_B+) @ G_{MAX}	+15 dBm
Continuous Power Dissipation	1.5W
θ_{JA} (Junction – Ambient)	+40°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+3°C/W
Operating Temperature Range (Case Temperature)	T_C = -40°C to +100°C
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s) .	+260°C

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Caution

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

TRUTH TABLE

Gain Set Target	Gain CodeWord	Code Name	Gain Set Target	Gain CodeWord	Code Name	Gain Set Target	Gain CodeWord	Code Name
20.0	000000	G_{20}	9.5	010101	$G_{9.5}$	-1.0	101010	G_{-1}
19.5	000001	$G_{19.5}$	9.0	010110	G_{9}	-1.5	101011	$G_{-1.5}$
19.0	000010	G_{19}	8.5	010111	$G_{8.5}$	-2.0	101100	G_{-2}
18.5	000011	$G_{18.5}$	8.0	011000	G_{8}	-2.5	101101	$G_{-2.5}$
18.0	000100	G_{18}	7.5	011001	$G_{7.5}$	-3.0	101110	G_{-3}
17.5	000101	$G_{17.5}$	7.0	011010	G_{7}	-3.5	101111	$G_{-3.5}$
17.0	000110	G_{17}	6.5	011011	$G_{6.5}$	-4.0	110000	G_{-4}
16.5	000111	$G_{16.5}$	6.0	011100	G_{6}	-4.5	110001	$G_{-4.5}$
16.0	001000	G_{16}	5.5	011101	$G_{5.5}$	-5.0	110010	G_{-5}
15.5	001001	$G_{15.5}$	5.0	011110	G_{5}	-5.5	110011	$G_{-5.5}$
15.0	001010	G_{15}	4.5	011111	$G_{4.5}$	-6.0	110100	G_{-6}
14.5	001011	$G_{14.5}$	4.0	100000	G_{4}	-6.5	110101	$G_{-6.5}$
14.0	001100	G_{14}	3.5	100001	$G_{3.5}$	-7.0	110110	G_{-7}
13.5	001101	$G_{13.5}$	3.0	100010	G_{3}	-7.5	110111	$G_{-7.5}$
13.0	001110	G_{13}	2.5	100011	$G_{2.5}$	-8.0	111000	G_{-8}
12.5	001111	$G_{12.5}$	2.0	100100	G_{2}	-8.5	111001	$G_{-8.5}$
12.0	010000	G_{12}	1.5	100101	$G_{1.5}$	-9.0	111010	G_{-9}
11.5	010001	$G_{11.5}$	1.0	100110	G_{1}	-9.5	111011	$G_{-9.5}$
11.0	010010	G_{11}	0.5	100111	$G_{0.5}$	-10.0	111100	G_{-10}
10.5	010011	$G_{10.5}$	0.0	101000	G_{0}	-10.5	111101	$G_{-10.5}$
10.0	010100	G_{10}	-0.5	101001	$G_{-0.5}$	-11.0	111110	G_{-11}
						-11.5	111111	$G_{-11.5}$

IDTF1240 SPECIFICATION

Specified values apply at V_{CC} = +5.0V, **f_{RF} = 200MHz**, T_C= +25°C,, V_{MODE} > V_{IH} (parallel mode), $STBY_A$, $STBY_B$ = 3.3V or NC, **R34 & R36 = 3.83K** unless otherwise noted. EVkit transformer losses are de-embedded

Parameter	Comment	Symbol	min	typ	max	units
Logic Input High		**V_{IH}**	2.0			V
Logic Input Low		**V_{IL}**	0		0.8	V
Logic Current	GA[5-0], GB[5-0] V_{IH} = 3.45 V, V_{IL} = 0V	**I_{IH}, I_{IL}**	***-2***		***+2***	µA
Logic Current[3]	V_{MODE}, STBY_A, STBY_B V_{IH} = 3.45 V, V_{IL} = 0V	**I_{IH}, I_{IL}**	***-10***		***+1***	µA
Temperature	Operating Case Temp Range	**T_{CASE}**		-40 to 100		degC
Voltage	All Supplies Operating Range	**V_{CC}**	4.75	5.00	5.25	V
Supply Current	Total, All V_{CC}	**I_{SUPP}**		***160***	***176***[1]	mA
Standby Current	Total, All V_{CC} ▪ STBY_A, STBY_B < V_{IL}	**I_{STBY}**		***2.3***	***5***	mA
Frequency Range	Low Distortion Range ▪ IP3O > 40 dBm, Pout +3 dBm/Tone ▪ Gain Set = G_{20}	**f_{RF}**		50 to 400		MHz
Frequency Range	Operating Range ▪ Gain > 17 dB ▪ With L1,L2,L3,L4 = 1500 nH	**f_{RF}**		5 to 560		MHz
1dB Gain Rolloff	Frequency @ 1dB Gain reduction vs. 100 MHz Gain	**BW**		400		MHz
Input Resistance[4]	Differential (> 10 dB RL)	**R_{IN}**		200		Ω
Output Resistance[4]	Differential (> 15 dB RL)	**R_{OUT}**		200		Ω
Maximum Gain		**G_{20} or G_{MAX}**	***18***	***20***		dB
Minimum Gain		**$G_{-11.5}$ or G_{MIN}**		***-11.5***	***-9***	dB
Minimum Gain Step	Parallel or Serial Mode	**LSB**		0.50		dB
Phase Error	Maximum phase change between G_{MAX} and any state down to G_{-4}	**IPE**		2.7		deg
Differential Gain Error	Between any two adjacent 0.5 dB steps	**DNL**		0.08		dB
Integral Gain Error	Error vs. line (G_{20} Ref)	**INL**		0.19		dB
Noise Figure	At G_{20}	**NF**		4.0	4.5[2]	dB
Noise Figure	At Gain Set = 10 dB (G_{10})	**NF_{BACK}**		5.3	5.8	dB
Output IP3 – Narrowband offset	▪ Set $G_{MAX,}$ ▪ Pout = +3 dBm per tone ▪ 800 KHz Tone Separation	**$IP3_{O1}$**	42	46.5		dBm
Output IP3 – Wideband offset	▪ Set $G_{MAX,}$ ▪ 20 MHz Tone Separation ▪ Pout = +3 dBm per tone	**$IP3_{O2}$**		45		dBm

IDTF1240 SPECIFICATION (CONT.)

Parameter	Comment	Symbol	min	typ	max	units
Output IP3 – Mid Gain	▪ Set Gain = 10 dB (G_{10}) ▪ Pout = +3 dBm per tone ▪ 800 KHz Tone Separation	**$IP3_{O3}$**	42	44.5		dBm
2nd Harmonic	▪ Set G_{10}, F_{RF} = 200 MHz ▪ Pout = +3 dBm	**H2**		-90		dBc
Output IP2	▪ Set G_{10}, F_{RF} = 190 MHz, 210 MHz ▪ Pout = +3 dBm per tone	**$IP2_H$**		76		dBm
1 dB Compression	Measure @ G_{20}	**$P1dB_O$**	***16***	***19.7***		dBm
Channel Isolation	OUT_B vs. OUT_A w/ IN_A input ▪ 200 MHz ▪ Measured @ G_{20} for both channels	**ISO_C**	60	69		dBc
Settling Time	▪ In Parallel Mode or In Serial Mode from CSb high ▪ Any two Adjacent 1dB Steps ▪ +/-0.10 dB Pout settling	**T_{1dB}**		12		nsec
Control Scheme	SPI™ (V_{MODE} = V_{IL} or GND) Parallel (V_{MODE} = NC or V_{IH})	**ctrl**		Both		
Serial Clock Speed	SPI 3 wire bus	**F_{CLOCK}**		***20***	***50***	MHz
Parallel to Serial Setup Time	Minimum Interval after V_{MODE} is pulled low to initiate serial programming via a CSb assertion	**T_{MODE}**		100		ns
Data to Clock Setup	Minimum Interval between valid data bit and Clock Rising Edge	**T_S**	***5***			ns
Data Hold Time	Minimum Interval after Clock Rising Edge that Data Bit must be held	**T_H**	***5***			ns
Clock to CSb Setup	CSb must be pulled low this minimum interval BEFORE the next rising clock edge	**T_{EN}**	***8***			ns
Clock Pulse Width	Minimum clock interval from rising to falling edge	**T_W**		15		ns

SPECIFICATION NOTES:

1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test

2 – All other Items in min/max columns are Guaranteed by Design Centering

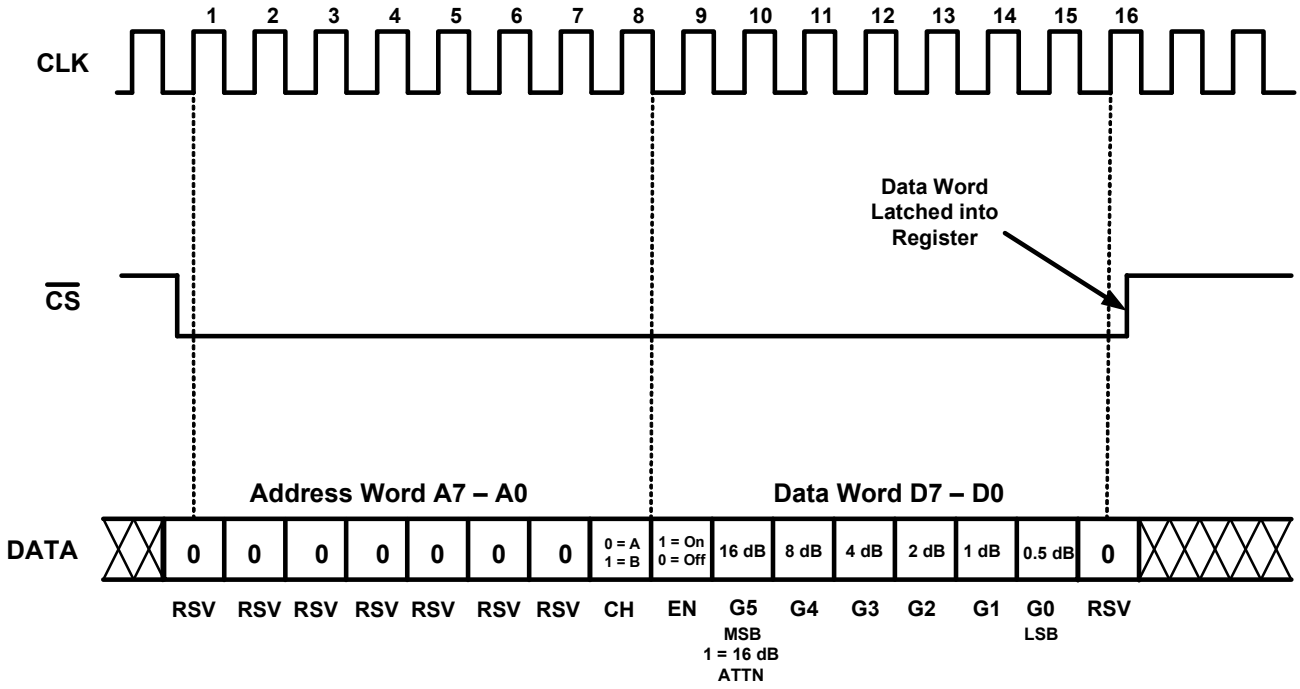
3 - VMODE, STBY_A, and STBY_B all have internal pullup resistors such that they float to > VIH

4 - Measured with 4:1 Transformers (see applications Circuit)

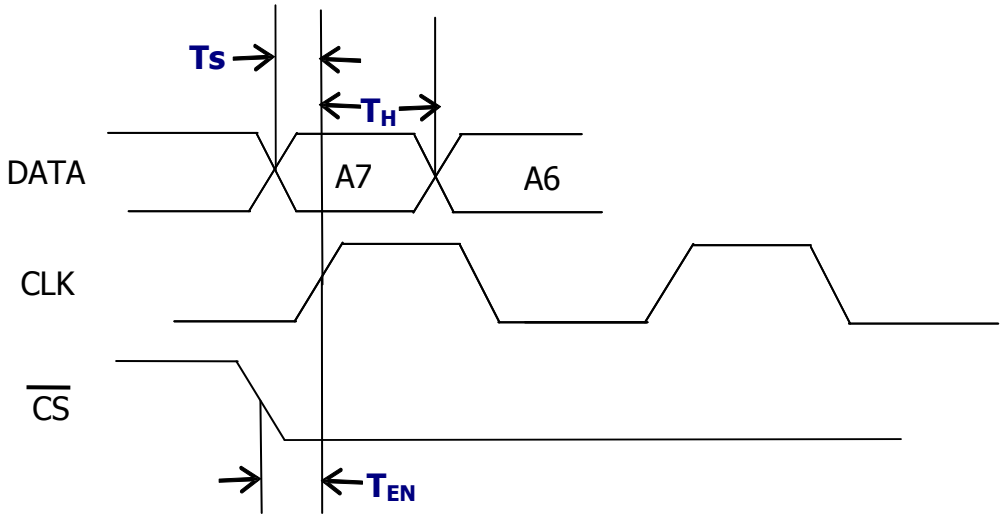
SERIAL MODE

Serial mode is selected by grounding V_{MODE} (pin4) or pulling it to a voltage < V_{IL}. In serial mode the IDTF1240 Ch_A and Ch_B gains can be programmed independently via the serial port by asserting Chip Select (CSb).

SERIAL MODE TIMING DIAGRAM HIGH LEVEL:

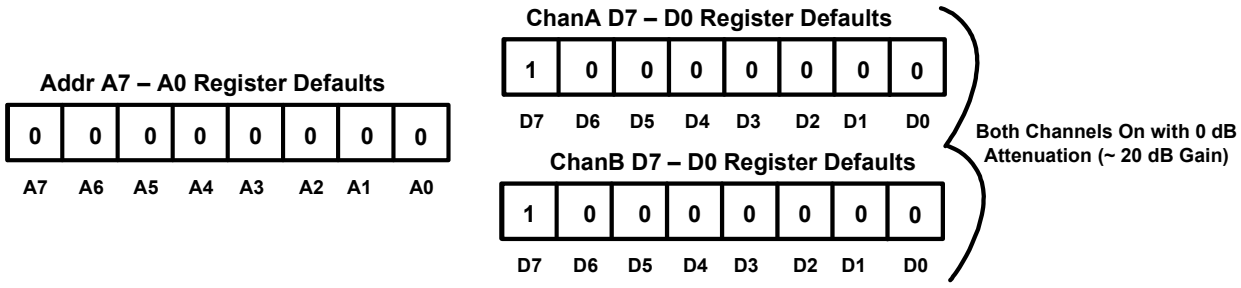


SERIAL MODE TIMING DIAGRAM ZOOM:



SERIAL MODE DEFAULT VALUES

Serial Register Default Values on Power Up. These apply to a hard reset when first applying V_{CC}.



SERIAL MODE ENABLE FUNCTIONS

Note that the STBY_A and STBY_B pins can be used in Serial mode for fast disable. These pins float high and can be left disconnected for serial operation. Alternately one can connect these pins to allow much faster enabling and disabling of the two VGA channels. Note the following:

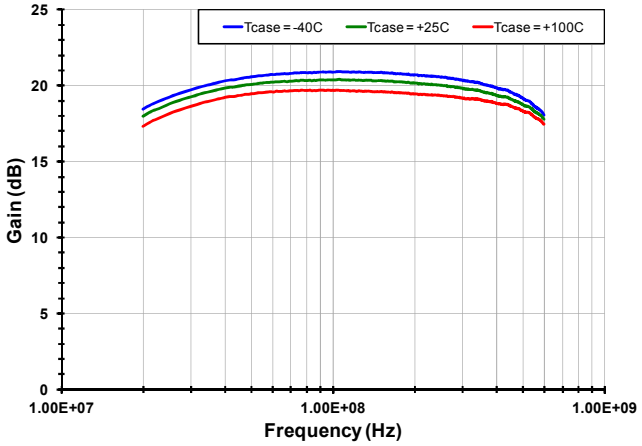
- When a VGA channel is disabled, the serial register will hold* the last enabled gain state.
- To enable a channel Serial D7 must be 1 AND the STBY pin must be high
- To disable a channel Serial D7 can be 0 OR the STBY pin can be low
- Through the Serial interface, **only the channel addressed by A0 will be enabled or disabled via D7**. For instance, to disable both Channel A and Channel B a serial programming cycle must be initiated and completed with A0 = 0 and D7 = 0 and then a 2nd serial programming cycle must be executed with A0 = 1 and D7 = 0.

***Note** – This does not apply when disabling through the Serial Bus. In this case, the gain value [D6 – D1] written during the subsequent Enable write replaces the Gain Setting. **For the Serial Disable write, the recommended Data Word is [01111110]**

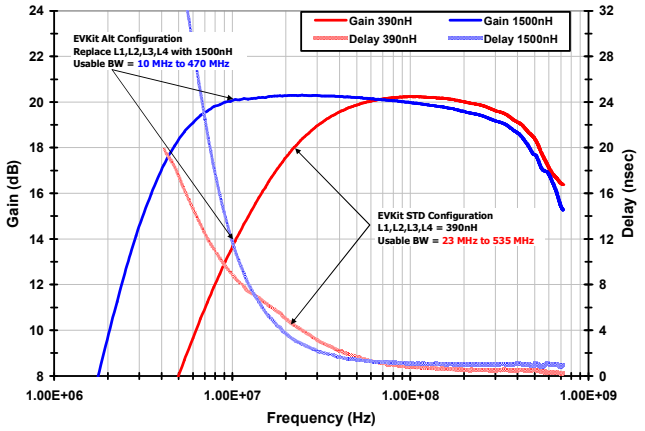
TYPICAL OPERATING CURVES (G_{MAX}, 5.00V, T_{CASE} = 25C, 200 MHz, TC4 de-embedded unless otherwise noted)

All temperatures are T_{CASE} unless noted as T_{AMB} or T_A = Ambient

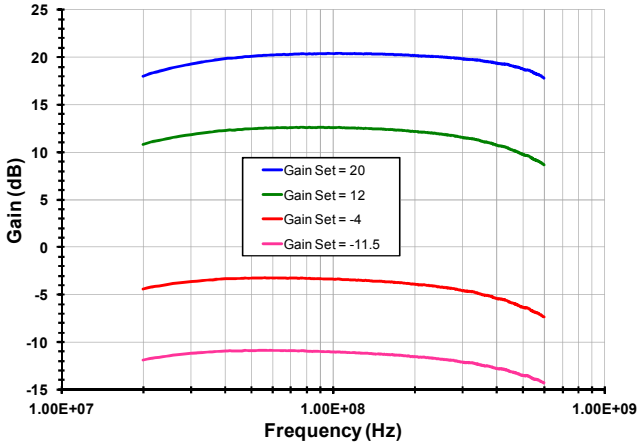
Gain vs. Frequency [Gain Set = 20 dB]



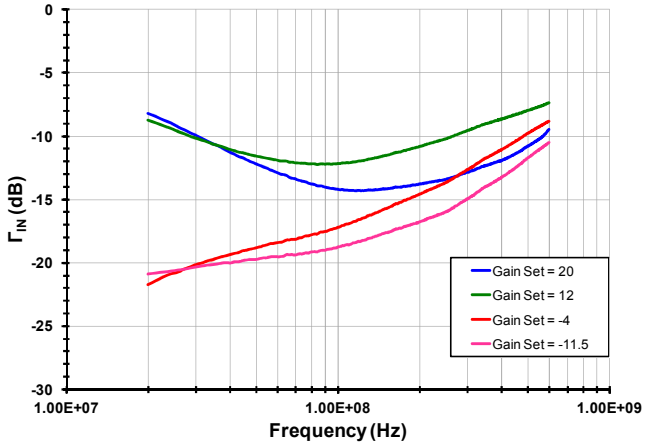
Extended Applications Range [T_{AMB} = 25C]



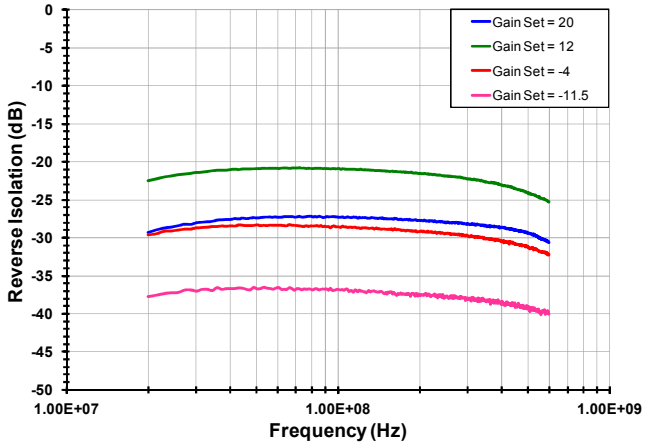
S_{21} vs. Frequency [T_{CASE} = 25C]



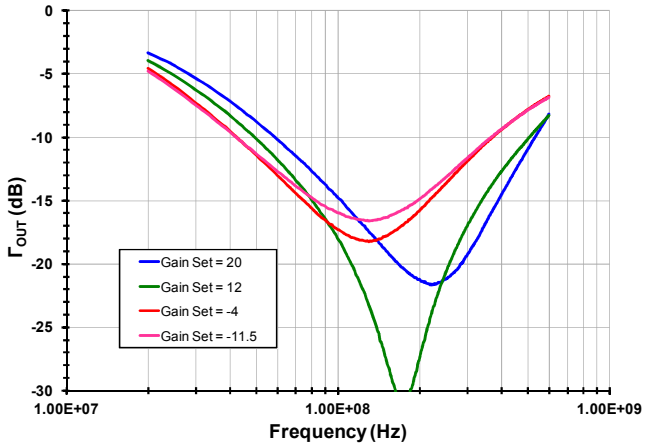
S_{11} vs. Frequency [T_{CASE} = 25C]



S_{12} vs. Frequency [T_{CASE} = 25C]

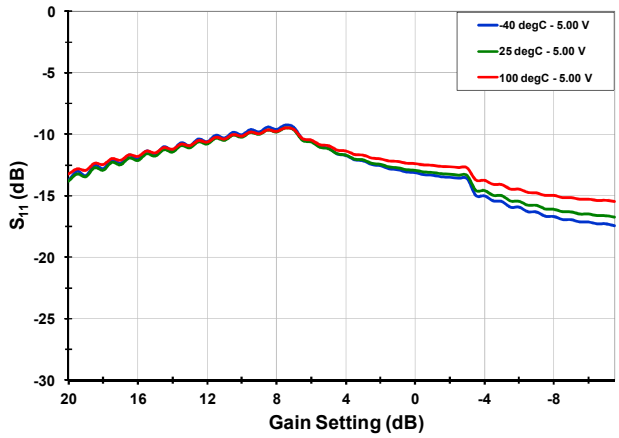


S_{22} vs. Frequency [T_{CASE} = 25C]

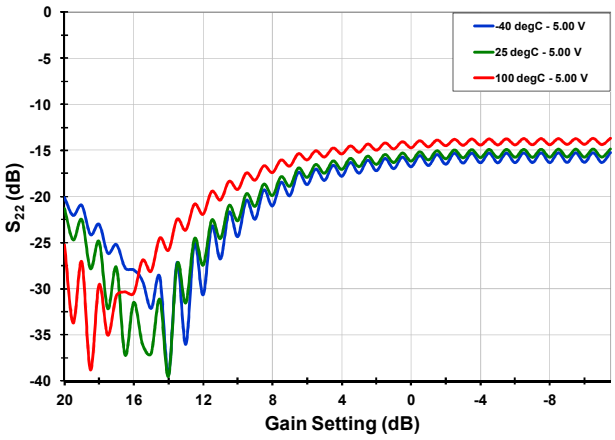


TOCs CONTINUED (-2-)

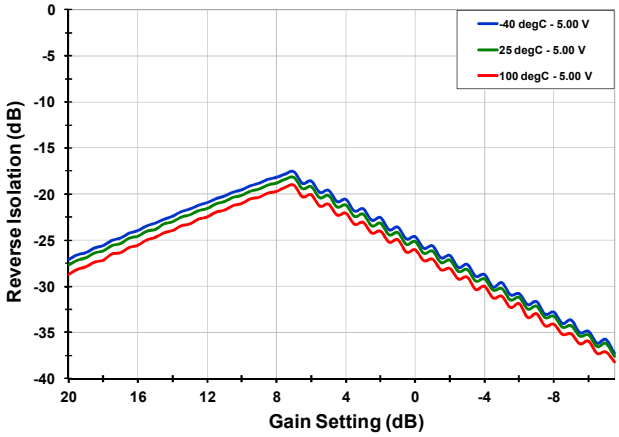
S_{11} vs. Gain Setting [200 MHz]



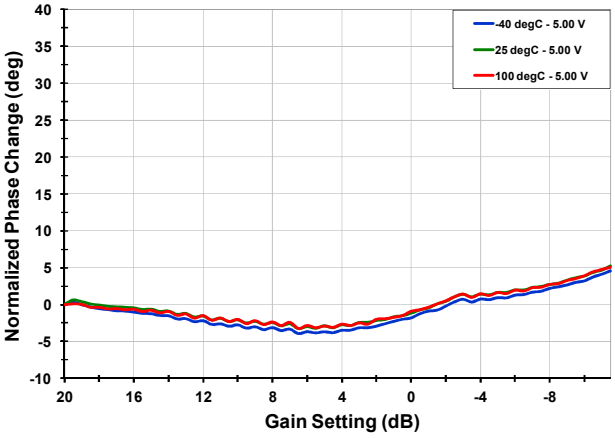
S_{22} vs. Gain Setting [200 MHz]



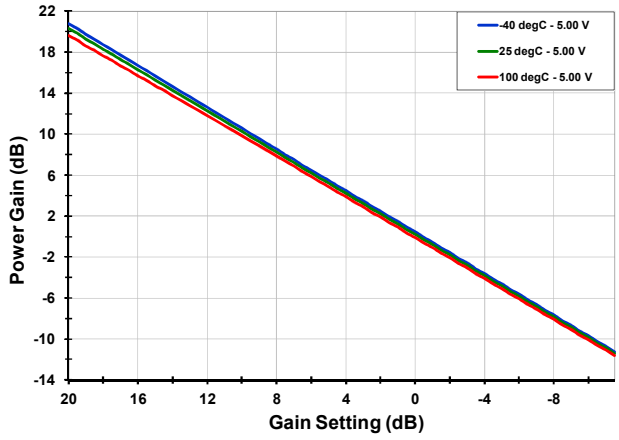
S_{12} vs. Gain Setting [200 MHz]



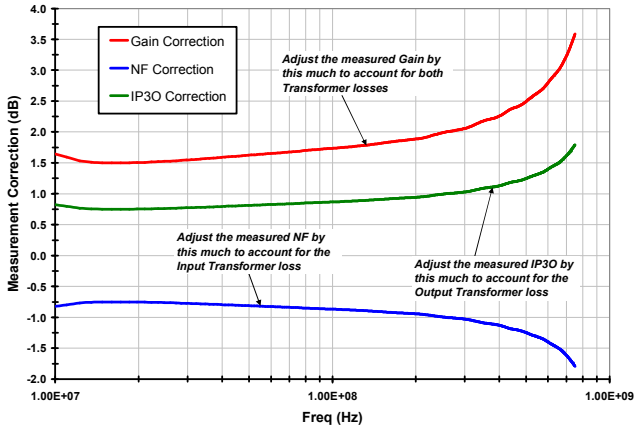
Phase Error vs. Gain Setting [200 MHz]



S_{21} vs. Gain Setting [200 MHz]

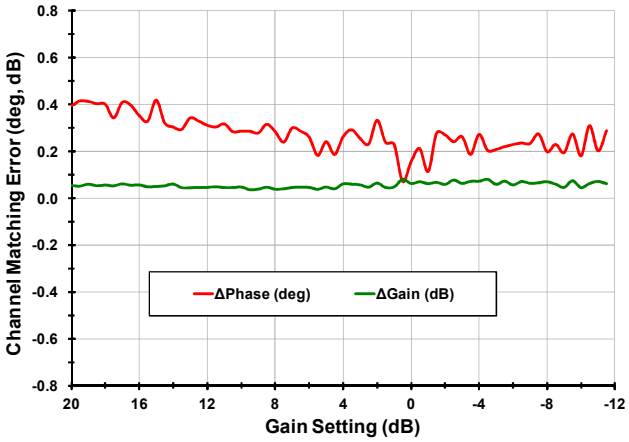


EVKit Measurement Corrections [TC4-1W, T_{AMB}]

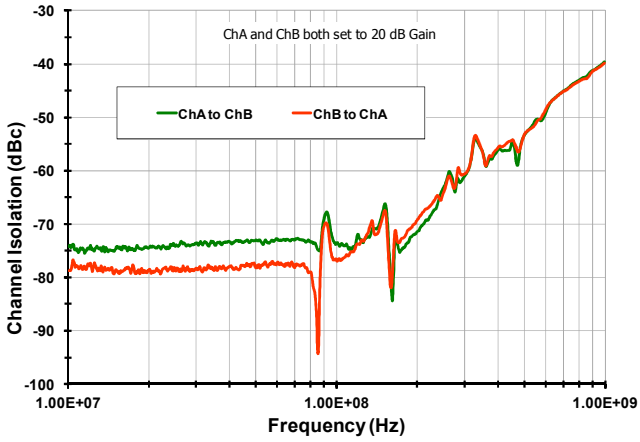


TOCs CONTINUED (-3-)

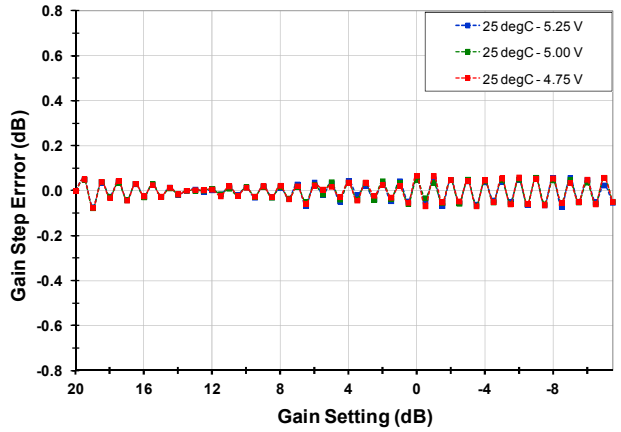
Channel Matching [200 MHz, T_{CASE} = 25C]



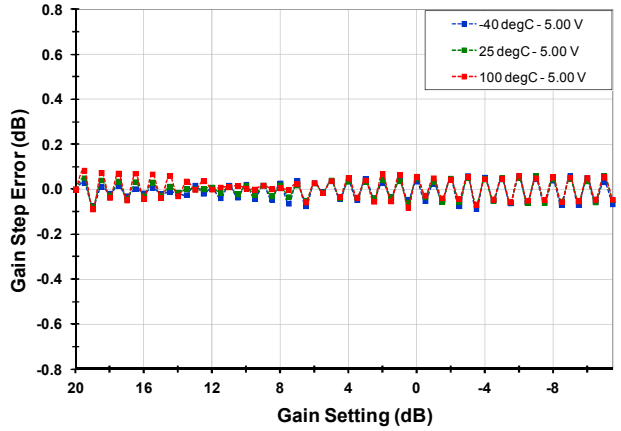
Channel Isolation vs. Frequency [T_{AMB} = 25C]



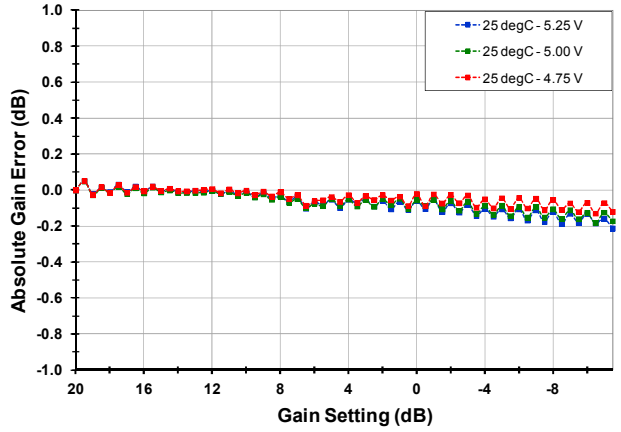
DNL vs. V_{CC} [200 MHz]



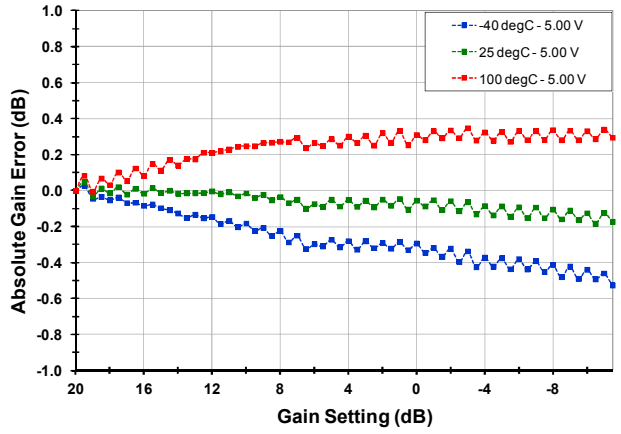
DNL vs. T_{CASE} [200 MHz]



INL vs. V_{CC} [200 MHz]

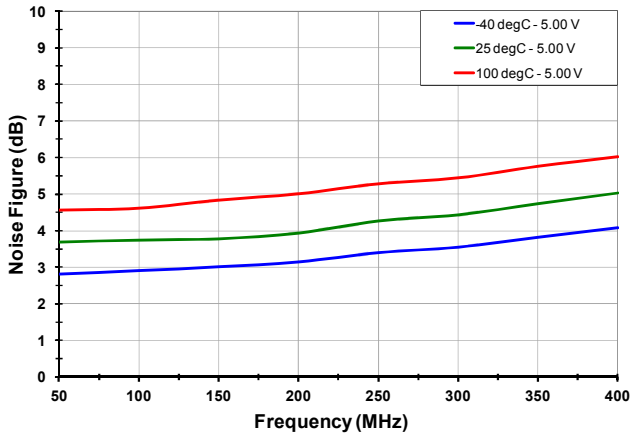


INL vs. T_{CASE} [200 MHz]

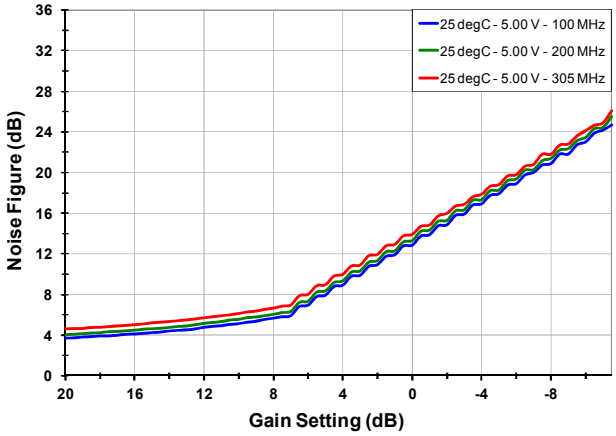


TOCs CONTINUED (-4-)

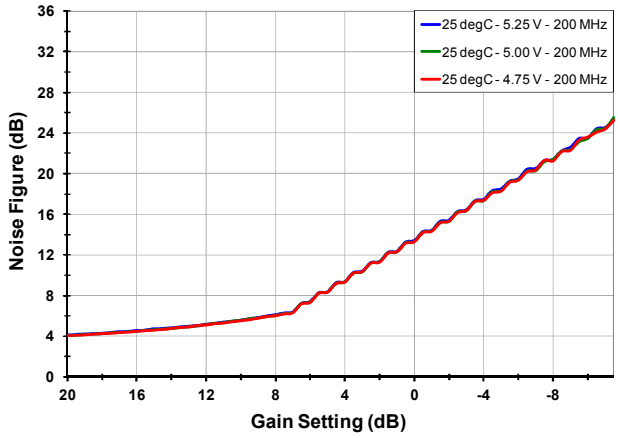
Noise Figure vs. Frequency [Gain Set = 20 dB]



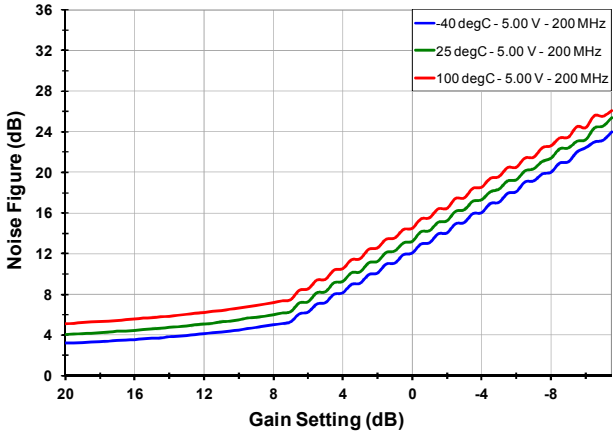
Noise Figure vs. Gain Setting [T_{CASE} = 25C]



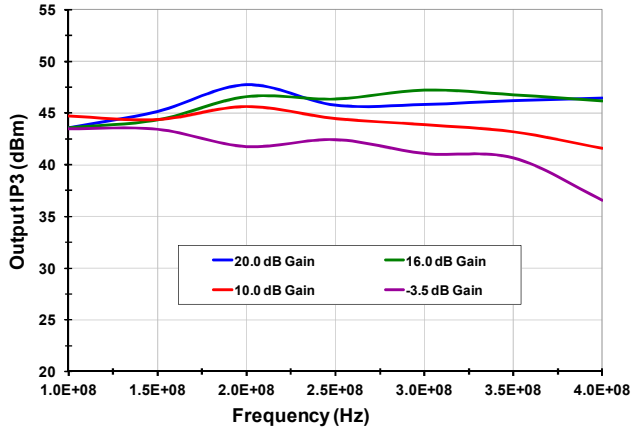
Noise Figure vs. V_{CC} [200 MHz]



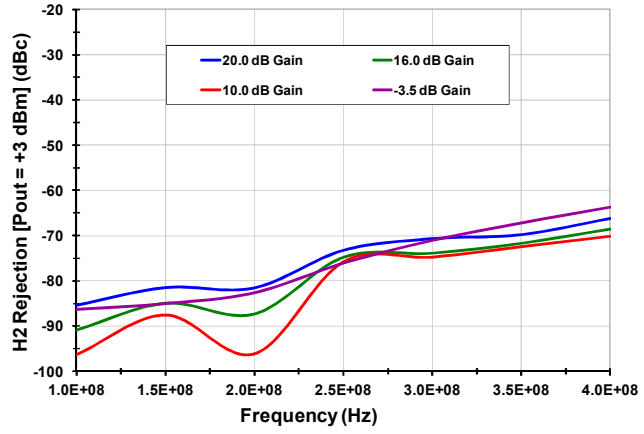
Noise Figure vs. T_{CASE} [200 MHz]



Output IP3 vs. Frequency [T_{CASE} = 25C]

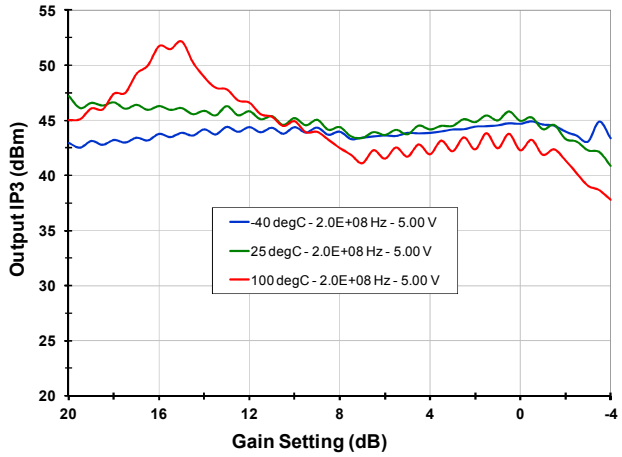


2nd Harmonic vs. Frequency [T_{CASE} = 25C]

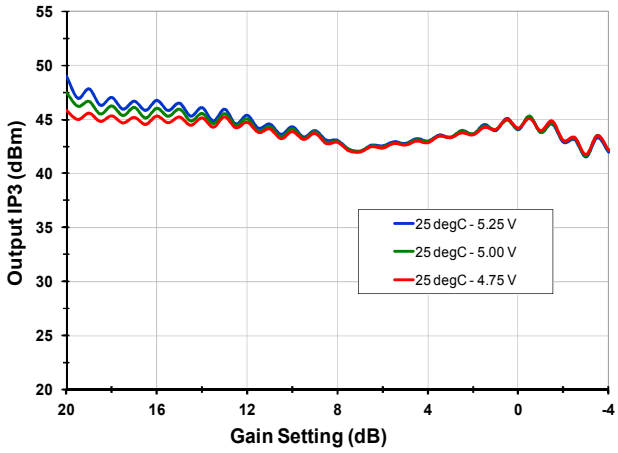


TOCs CONTINUED (-5-)

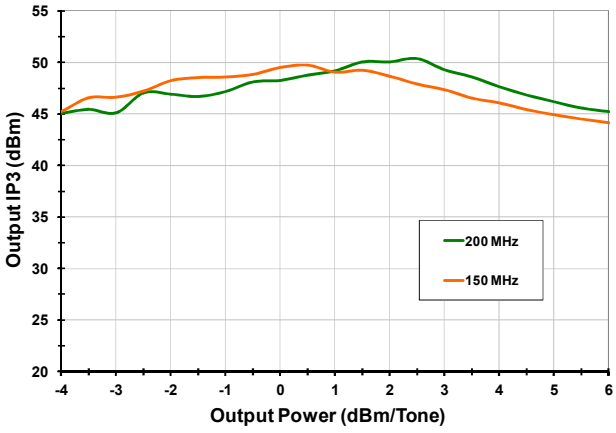
Output IP3 vs. T_{CASE} [200 MHz]



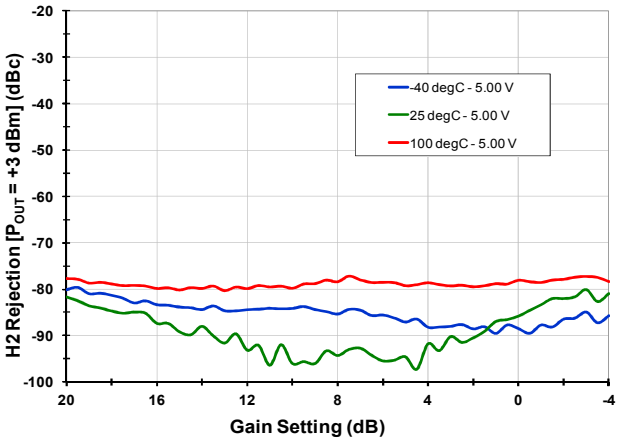
Output IP3 vs. V_{CC} [200 MHz]



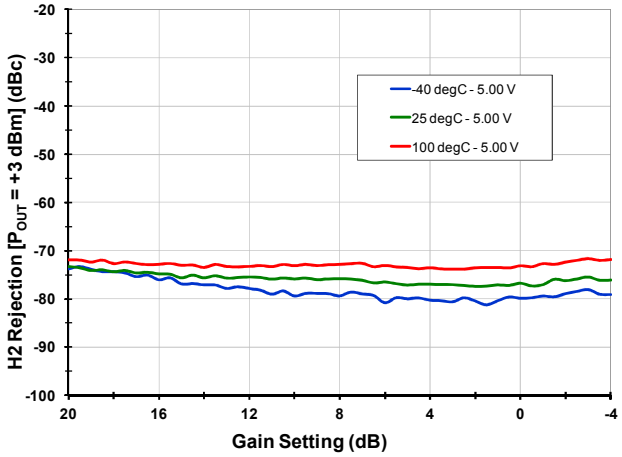
Output IP3 vs. Pout [T_{AMB} = 25C, Gain Set = 20 dB]



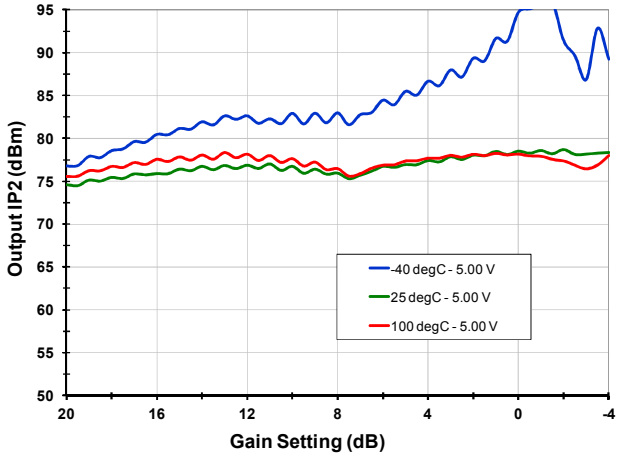
2nd Harmonic vs. T_{CASE} [200 MHz]



2nd Harmonic vs. T_{CASE} [250 MHz]

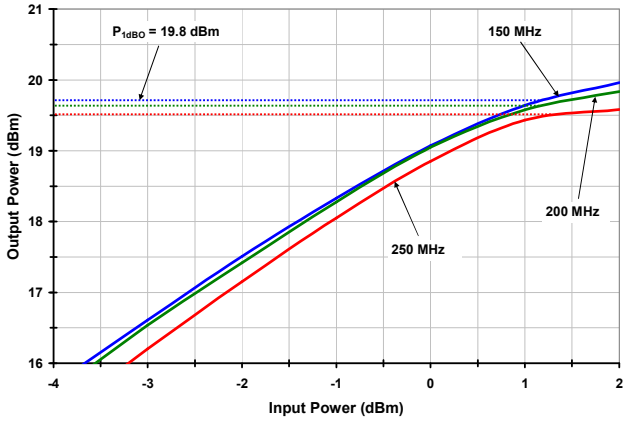


Output IP2 vs. T_{CASE} [200 MHz]

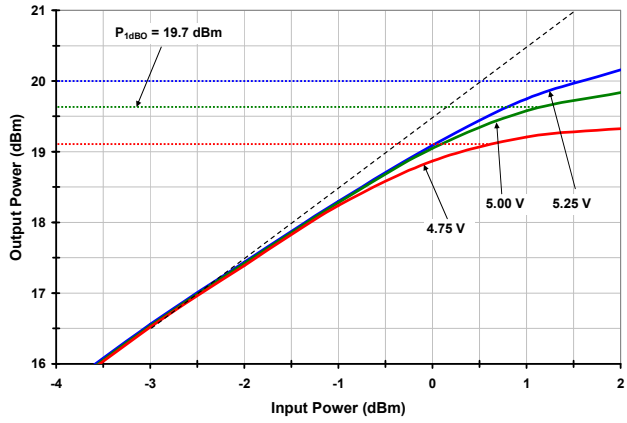


TOCs CONTINUED (-6-)

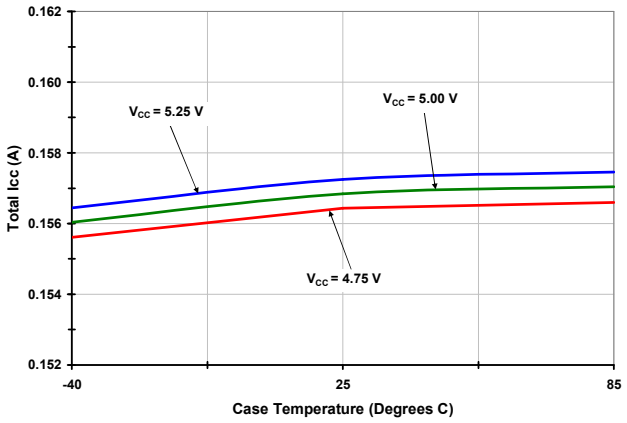
Gain Compression vs. Frequency [T_{AMB} = 25C]



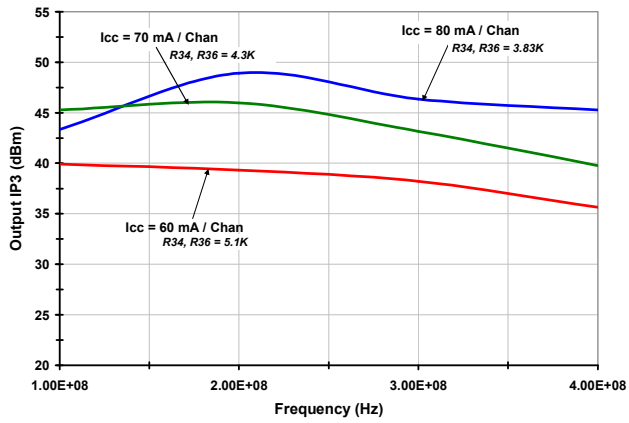
Gain Compression [200 MHz, T_{AMB} = 25C]



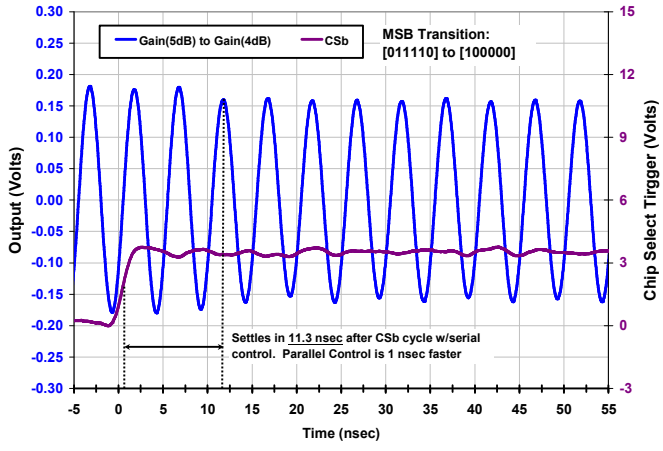
I_{CC} vs. T_{CASE}



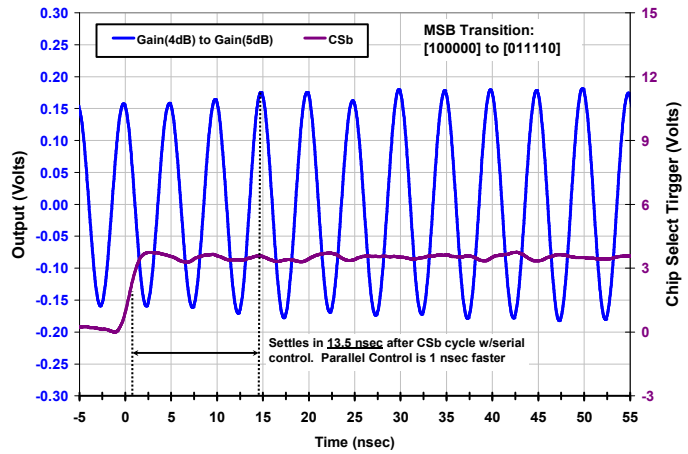
Output IP3 vs. I_{CC} [T_{AMB} = 25C]



Settling Time (1dB Step, 200 MHz, MSB+)



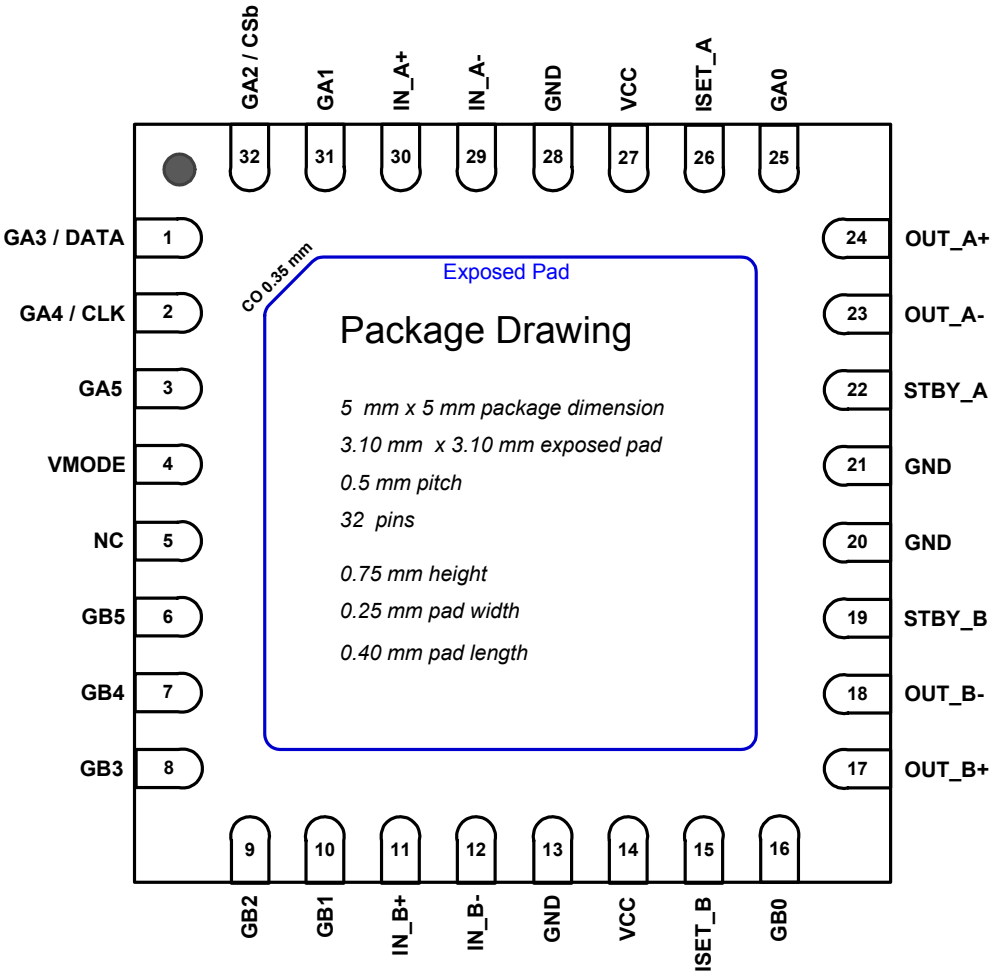
Settling Time (1dB Step, 200 MHz, MSB-)



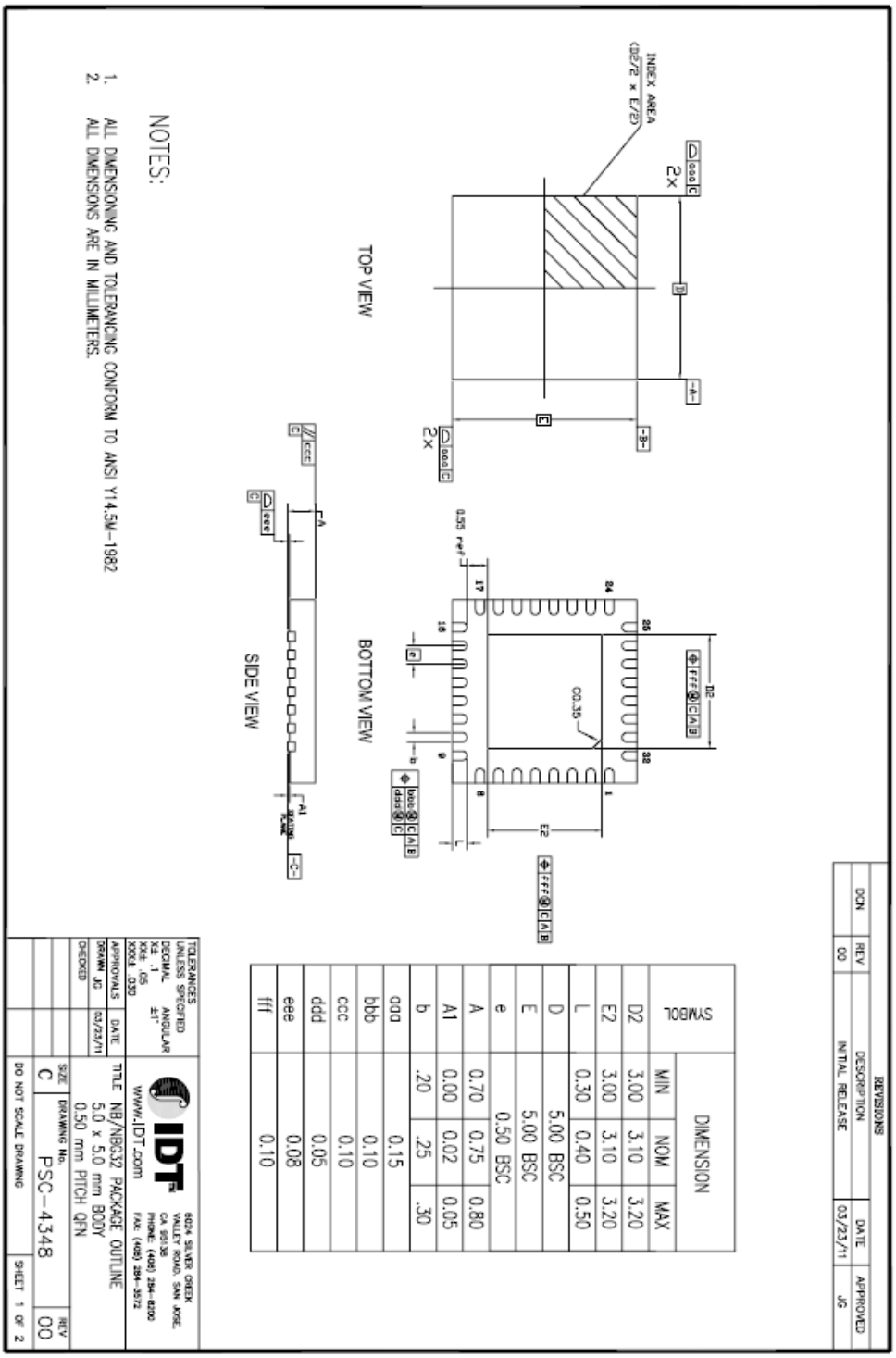
PIN DIAGRAM (F1240 – COMPATIBILITY W/LMH DEVICES)

Note: VMODE, STBY_A, and STBY_B have internal Pullup resistors

TOP View
(looking through the top of the package)



PACKAGE DRAWING

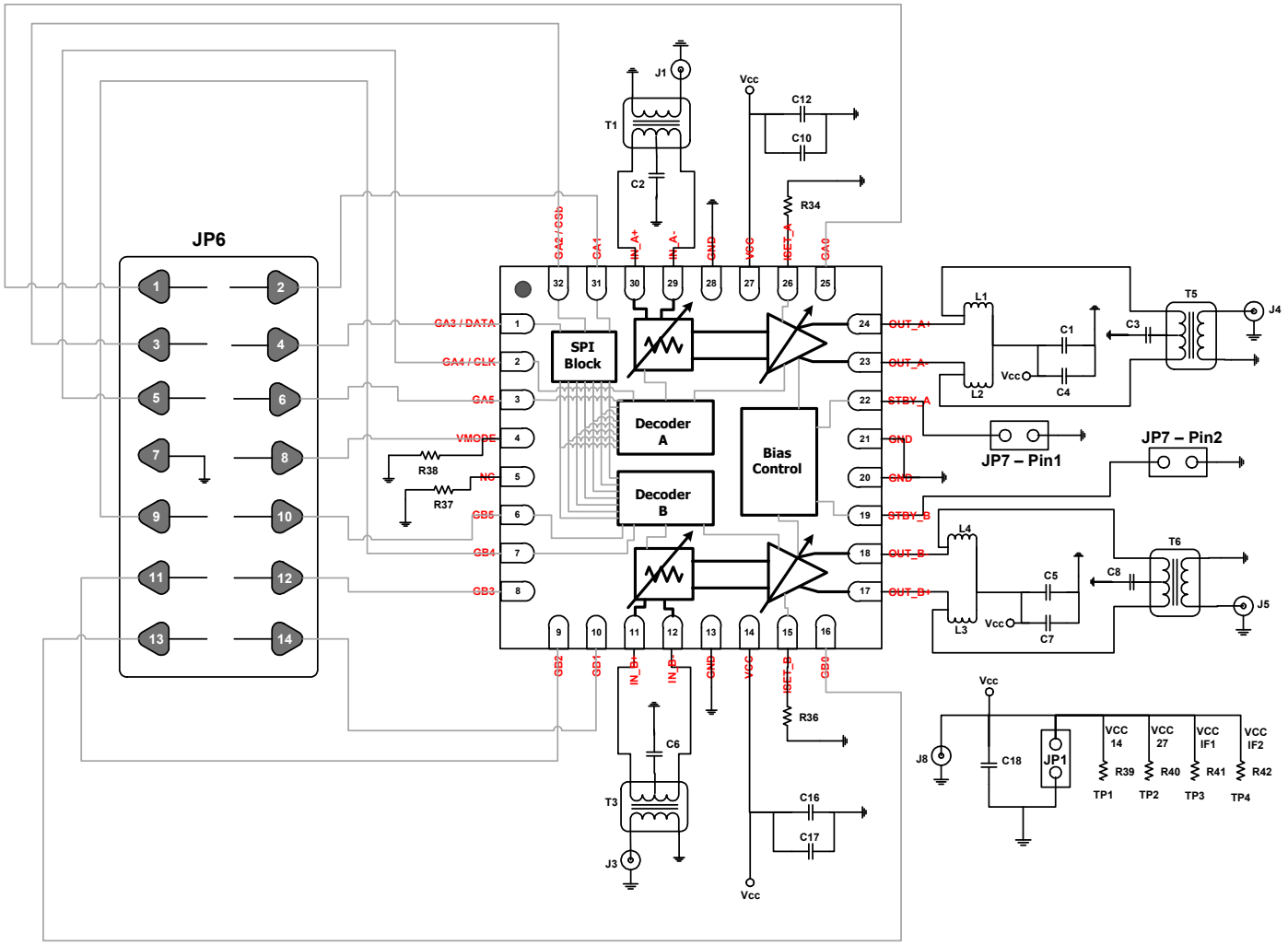


PIN DESCRIPTIONS

Pin #	Pin Name	Pin Function
1	GA3 / DATA	4 dB ATTN ctrl bit for Channel A (Parallel Mode) OR DATA (Serial Mode)
2	GA4 / CLK	8 dB ATTN ctrl bit for Channel A(Parallel Mode) OR CLK (Serial Mode)
3	GA5	16 dB Attenuation ctrl bit for Channel A
4	VMODE	Pull low for serial mode. Float or pull high for parallel mode. Has internal Pullup
5	NC	This pin is internally grounded
6	GB5	16 dB Attenuation ctrl bit for Channel B: 1 or high = 16 dB ATTN
7	GB4	8 dB Attenuation ctrl bit for Channel B: 1 or high = 8 dB ATTN
8	GB3	4 dB Attenuation ctrl bit for Channel B: 1 or high = 4 dB ATTN
9	GB2	2 dB Attenuation ctrl bit for Channel B: 1 or high = 2 dB ATTN
10	GB1	1 dB Attenuation ctrl bit for Channel B: 1 or high = 1 dB ATTN
11	IN_B+	Channel B Differential Input +. AC couple
12	IN_B-	Channel B Differential Input -. AC couple
13	GND	Connect this pin to Ground
14	VCC	Connect this pin to the 5V DC Power Bus
15	ISET_B	ChB Icc set: Use the recommended value from the BOM section
16	GB0	0.5 dB Attenuation ctrl bit for Channel B: 1 or high = 0.5 dB ATTN
17	OUT_B+	Channel B Differential Output +. Pull up to Vcc through an inductor
18	OUT_B-	Channel B Differential Output-. Pull up to Vcc through an inductor
19	STYB_B	Pull low to Power Down ChB. Float or Pull high to enable ChB
20	GND	Connect this pin to Ground
21	GND	Connect this pin to Ground
22	STYB_A	Pull low to Power Down ChA. Float or Pull high to enable ChA
23	OUT_A-	Channel A Differential Output -. Pull up to Vcc through an inductor
24	OUT_A+	Channel A Differential Output +. Pull up to Vcc through an inductor
25	GA0	0.5 dB Attenuation ctrl bit for Channel A
26	ISET_A	ChA Icc set: Use the recommended value from the BOM section
27	VCC	Connect this pin to the 5V DC Power Bus
28	GND	Connect this pin to Ground
29	IN_A-	Channel A Differential Input -. AC couple
30	IN_A+	Channel B Differential Input +. AC couple
31	GA1	1 dB Attenuation ctrl bit for Channel A
32	GA2 / CSb	2 dB ATTN ctrl bit for Channel A (Parallel Mode) OR chip select (Serial Mode)
EP	Exposed Paddle	Connect to Ground with multiple vias for good thermal relief

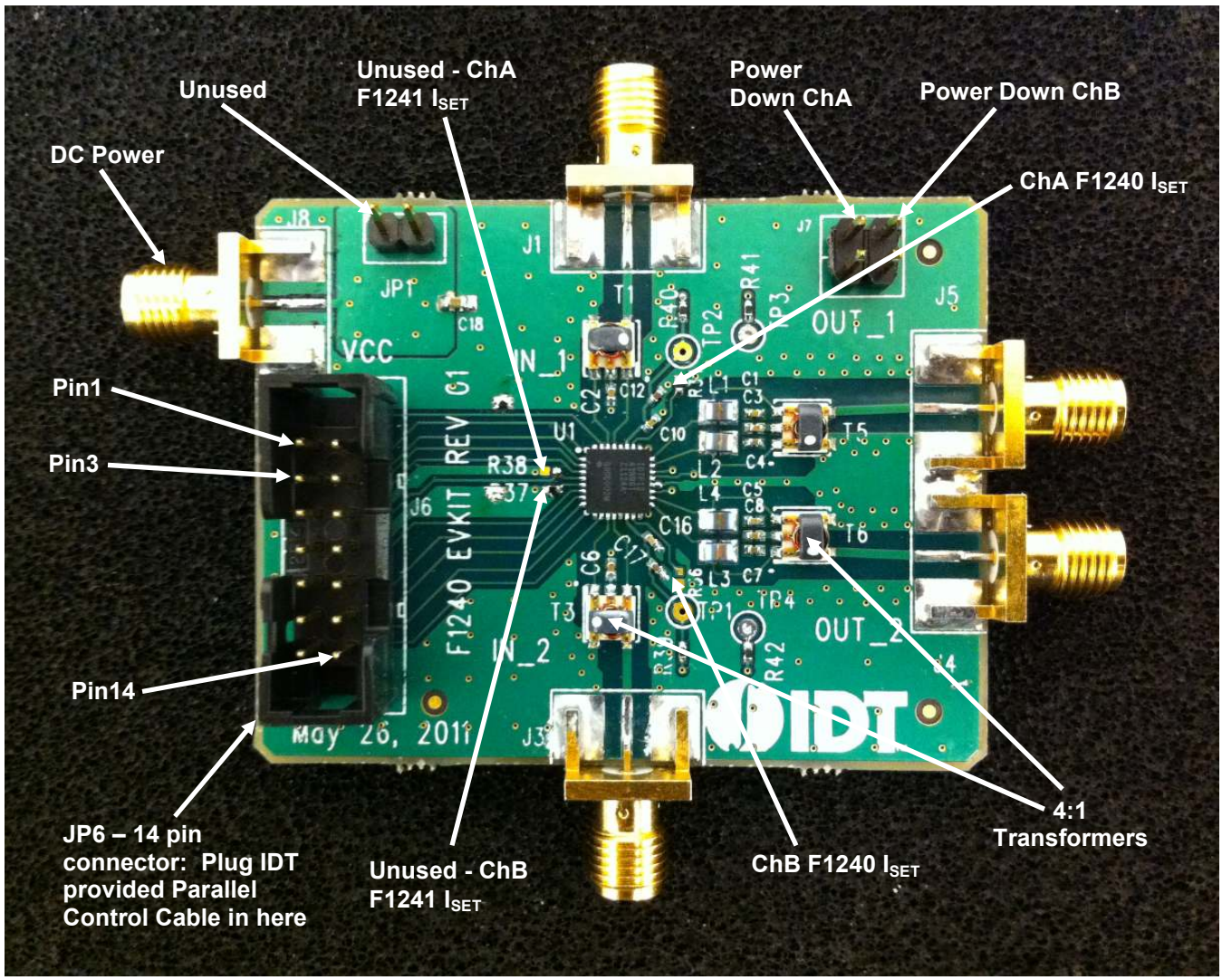
EVKIT SCHEMATIC

The diagram below describes the recommended applications / EVkit circuit:



EVKIT OPERATION (Email: RFsupport@IDT.com to request an EVkit and Control Cable)

The picture and graphic below describe how to operate the EVkit



EVKIT BOM (F1240)

REF DES	VALUE	CASE SIZE	MFG		REF DES	VALUE	CASE SIZE	MFG
R34	3.83K +/-1%	0402			C7	0.1 uF	0402	
R36	3.83K +/-1%	0402			C8	0.1 uF	0402	
R37	0 ohm	0402			C10	1,000 pF	0402	
R38	DNP	0402			C12	0.1 uF	0402	
R39	0 ohm	0402			C16	1,000 pF	0402	
R40	0 ohm	0402			C17	0.1 uF	0402	
R41	0 ohm	0402			C18	10 uF	0603	
R42	0 ohm	0402			T1	4:1	TC4-1WG2+	MiniCircuits
L1	390 nH	0805	Coilcraft		T3	4:1	TC4-1WG2+	MiniCircuits
L2	390 nH	0805	Coilcraft		T5	4:1	TC4-1WG2+	MiniCircuits
L3	390 nH	0805	Coilcraft		T6	4:1	TC4-1WG2+	MiniCircuits
L4	390 nH	0805	Coilcraft		J1	SMA		
C1	1,000 pF	0402			J3	SMA		
C2	0.1 uF	0402			J4	SMA		
C3	0.1 uF	0402			J5	SMA		
C4	0.1 uF	0402			J8	SMA		
C5	1,000 pF	0402			JP1	DNP		
C6	0.1 uF	0402			J6	14 pin- CTRL		
					J7	4 pin - STBY		

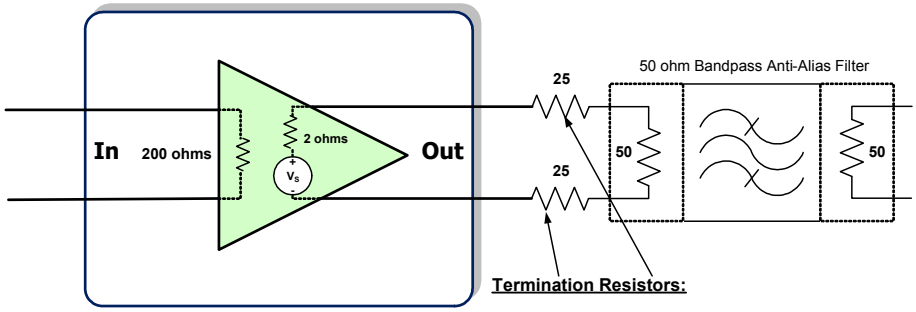
APPLICATIONS INFORMATION

The F1240 has been optimized for use in high performance IF sub-sampling applications. They have unique features that make them ideal for these very demanding applications.

Matched Output

Unlike competing devices the F1240 features a matched 200 ohm differential output. All of the datasheet parameters are specified as such. For instance, the Gain of 20 dB is a true Transducer Power gain (Power delivered to the matched load minus Power available from the source). This is in contrast to competing devices that usually have a high or low impedance output and must be terminated with resistors to operate properly. In IF sampling applications, the IF VGA usually drives a Bandpass anti-alias filter which precedes the ADC. These filters typically need to 'see' matched terminations. Only the F1240's performance is preserved in this environment. See directly below for a comparison to popular VGA styles.

Example 1: 'Voltage Mode' VGA



Must Adjust Datasheet Values:

Gain with 100 ohm load = 22 dB
True **Gain in-system = 19 dB**

Output IP3 with 100 ohm load = +44 dBm
True **IP3O in-system = +41 dBm**

Termination Resistors:

Ensure BPF is terminated properly with 50 ohms

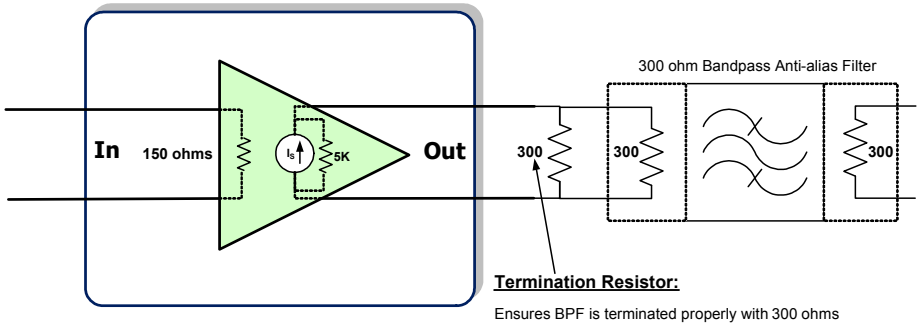
Total load = 100 ohms.....Available Power = V^2_S / 100

Half the Power is dissipated in the terminating resistors: $(0.5V_S)^2$ / 50

The other half of the power is delivered to the input of the BPF

Effectively, the Gain drops by **3 dB**

Example 2: 'Current Mode' VGA



Must Adjust Datasheet Values:

Gain with 150 ohm load = 19 dB
True **Gain in-system = 16 dB**

Output IP3 with 150 ohm load = +46 dBm
True **IP3O in-system = +43 dBm**

Termination Resistor:

Ensures BPF is terminated properly with 300 ohms

Total load = 150 ohms...Available Power = I^2_S X 150

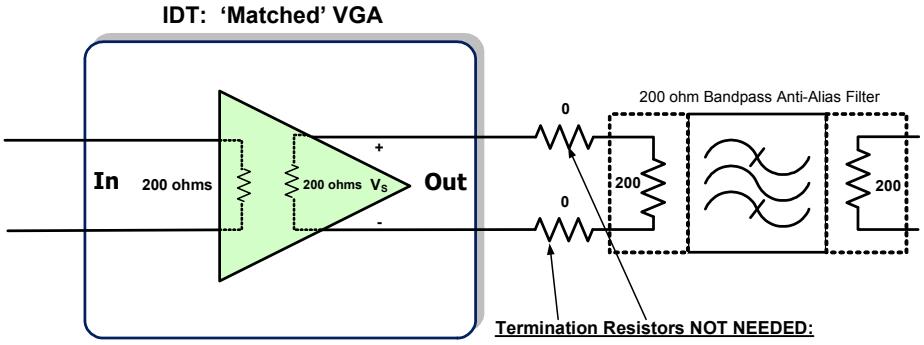
Half the Power is dissipated in the terminating resistor: $(0.5I_S)^2$ X 300

The other half of the power is delivered to the BPF

Again Effectively, the Gain drops by **3 dB**

APPLICATIONS INFORMATION (CONT.)

Matched Output (cont.)



NO NEED to Adjust Datasheet Values:

Gain with 200 ohm load = 20 dB
True **Gain in-system = 20 dB**

Output IP3 with 200 ohm load = +49 dBm
True **IP3O in-system = +49 dBm**

Termination Resistors NOT NEEDED:

VGA itself terminates BPF with proper Z = 200

Total external load = 200 ohms

Available Power = V^2_S / 200

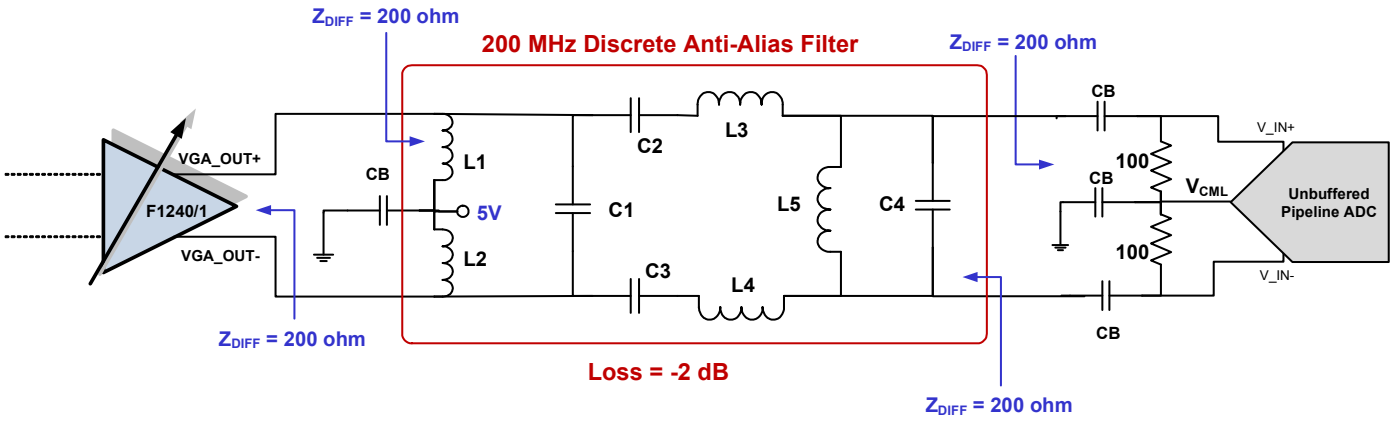
ALL of the power is delivered to the input of the BPF

Effectively, the **Gain is unchanged!**

Noise Contour

The remarkable FlatNoise™ feature of the device (see first four graphs on page 10) has great benefits when implemented in wideband multi-carrier systems. For the first 13 dB of attenuation range, the device has only 2.3 dB degradation in noise figure. This is in stark contrast to standard VGAs like the voltage or current mode devices described earlier. These devices have a linear dB-for-dB degradation in Noise Figure with increasing attenuation.

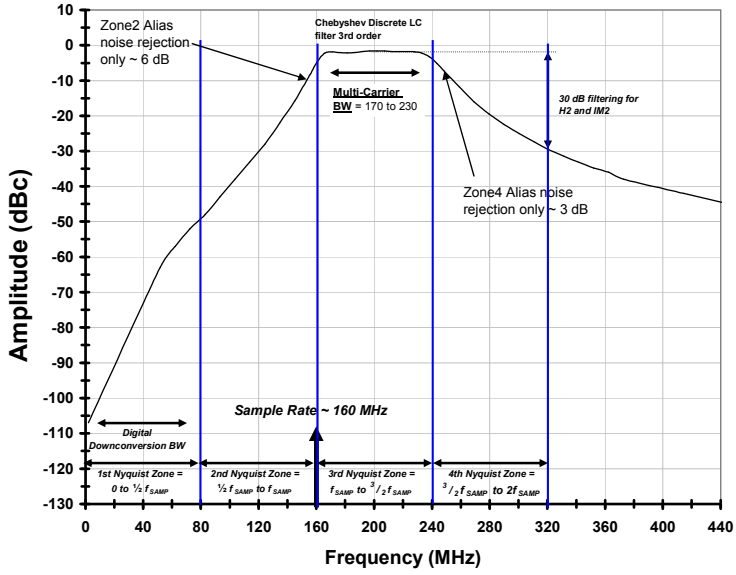
Refer to the figure below. It depicts the F1240 driving a matched Anti-Alias Filter which is followed by an ADC with a differential resistive 200 ohm termination. Note that at each point in the system the matching is preserved.



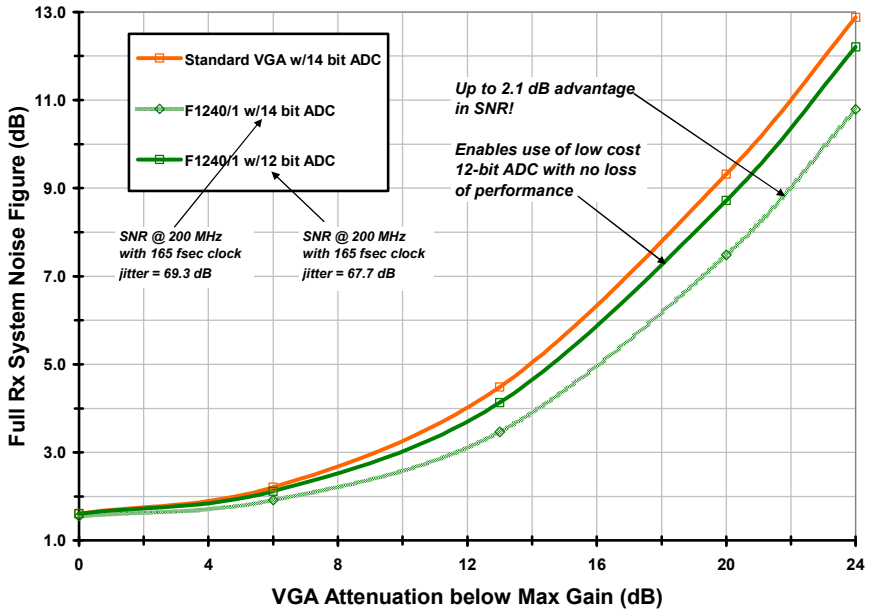
APPLICATIONS INFORMATION (CONT.)

Noise Contour (cont.)

A discrete realization of a 3rd order Anti-Alias filter is shown below. Sampling occurs in Nyquist Zone3 for a 60 MHz multi-carrier signal. Noise just 20 MHz above & below the signal bandedges will alias from either Zone4 or Zone2 and show up as added noise in the desired band at the digital output of the ADC.



The result is that the F1240 with it's unique noise contour will improve SNR significantly in this multi-carrier instance . Note in the graph below: **SNR improves over 2 dB** at high attenuation settings which potentially allows for the use of a lower cost 12-bit ADC in the Rx path.



APPLICATIONS INFORMATION (CONT.)

Other Key Features:

Current Setting Resistors – The IDTF1240 already offers the best IM3 distortion performance over the widest Power range when driving a matched load w/ 160 mA Total I_{CC}. The user has the option to reduce I_{CC} even further at the expense of Output IP3. See the graph at Middle Right on Page 12 for details. Note that ChA and ChB I_{CC} can be independently set.

Settling Time – The IDTF1240 has been optimized to settle quickly and smoothly without any 'glitching' when changing gain between **ANY** adjacent steps. Note the two graphs at the bottom of Page 12. Even for 1 dB steps that involve **MSB transitions** the settling time is still <15 nsec.

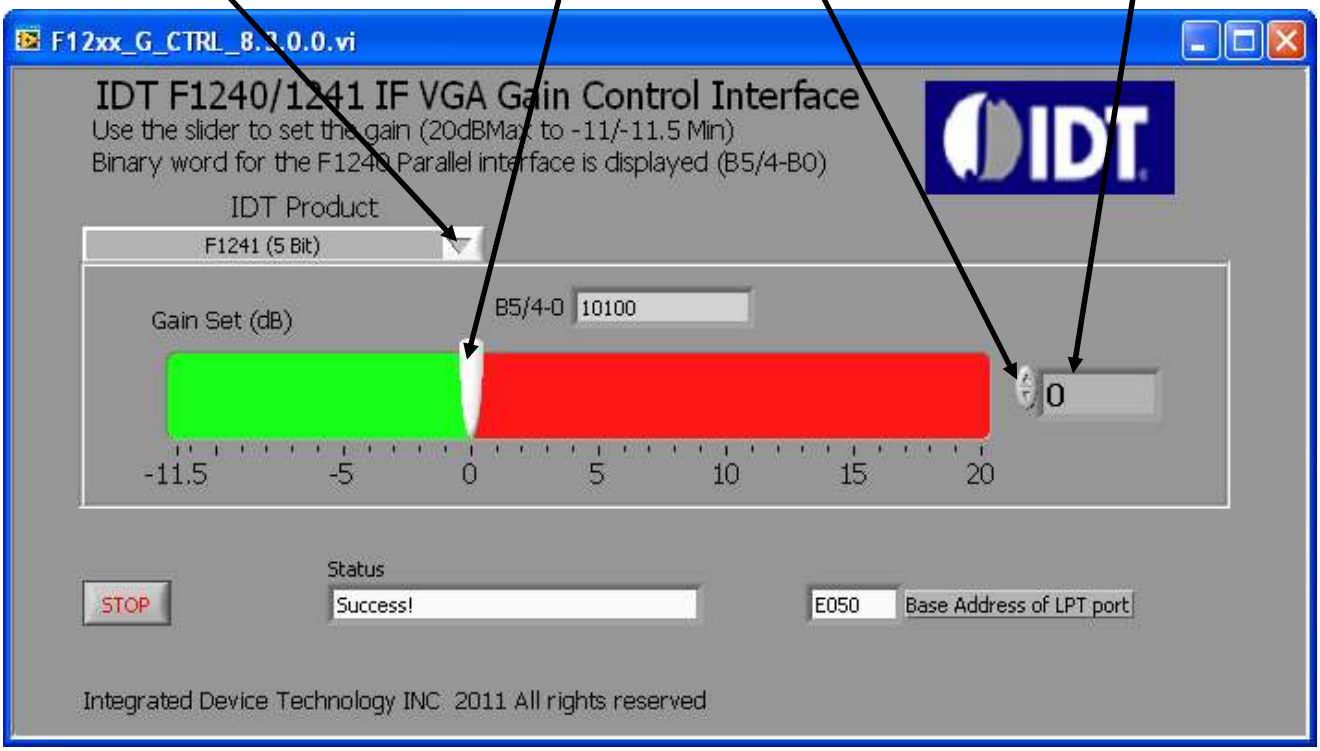
Gain Controller Software

Pulldown to select F1240 (6 bit ctrl) or F1241 (5 bit ctrl)

Slide to Set Gain for Both ChA and ChB

Scroll to Adjust Gain Value

Type Gain value in here



Connect IDT Cable to 14 pin connector on EVkit

Connect IDT Cable to 'Parallel Port' of Desktop PC

Download Controller Software:

- Point your browser to: ftp3.idt.com
- User Name: prodemo
- Password: Fa9HsG2I
- File Name: F12xx_G_CTRL_8.4.2.0.zip
- Run setup.exe right from the zip file…

Contact your IDT Sales Professional or Email: RFsupport@IDT.com to request applications support

APPLICATIONS INFORMATION (CONT.)

Operation into a 100 ohm load

The F1240 can be dropped directly into a 100 ohm termination environment without any topology changes, so no board redesign is necessary. The example schematic below is for a 153 MHz IF center frequency. Simply replace the pullup inductors already on the board with 91 nH and replace the series AC coupling capacitors already on the board with 18 pF. The F1240 in this case will then drive a 100 ohm filter with ~16 dB return loss. See schematic and measured results when matched to 100 ohms below: