MP8126

550mA, 8V-to-14V Input, LNB-Power Supply and Control-Voltage Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP8126 is a voltage regulator designed to provide efficient, low-noise power to a satellite receiver's RF LNB (Low Noise Block) converter. It connects using a coaxial cable through a link that is compatible with the European EUTELSAT specification (DiSEqC) 1.x that receives instructions from a dedicated controller.

The MP8126 integrates a current-mode boost regulator followed by a tracking linear regulator. The boost regulator provides a clean and quiet power source that will not contaminate the low-noise RF signal as it is down-converted to the receiver. The tracking linear regulator protects the output against overloads or shorts.

The MP8126 provides a number of features described in the DiSEqC, including voltage selection of horizontal or vertical LNB polarization directions, and selectable VOUT compensation for substantial voltage drops on long coaxial cable. In accordance with DiSEqC, the part can detect a 22kHz signal and output a shaped signal.

The MP8126 is available in a thermally-enhanced TSSOP16EP and 24-pin QFN (4X4mm) packages.

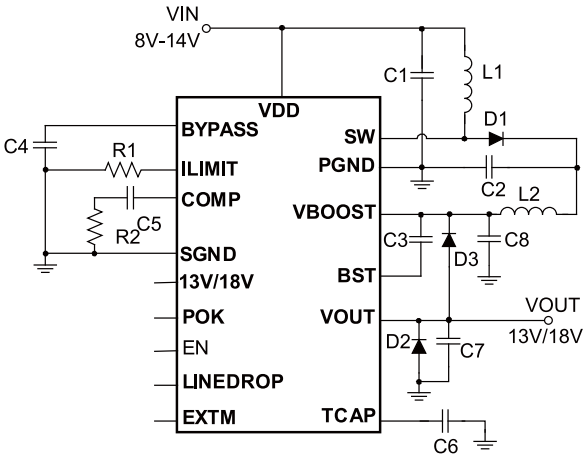
FEATURES

- DiSEqC 1.x Compatibility
- Up to 550mA Output Current
- Programmable Current Limit
- 8V-to-14V Input Voltage
- Boost Converter with Internal Switch
- Low-Noise LDO Output
- Built-In 22kHz Signal Shaper
- 1V Line-Drop Compensator
- Adjustable Soft-Start Time
- POK Indicator
- Short-Circuit Protection
- Over-Temperature Protection
- TSSOP16 Exposed Pad and 24-pin QFN (4X4mm) Packages

APPLICATIONS

- LNB Power Supply and Control for Satellite Set Top Boxes

TYPICAL APPLICATION

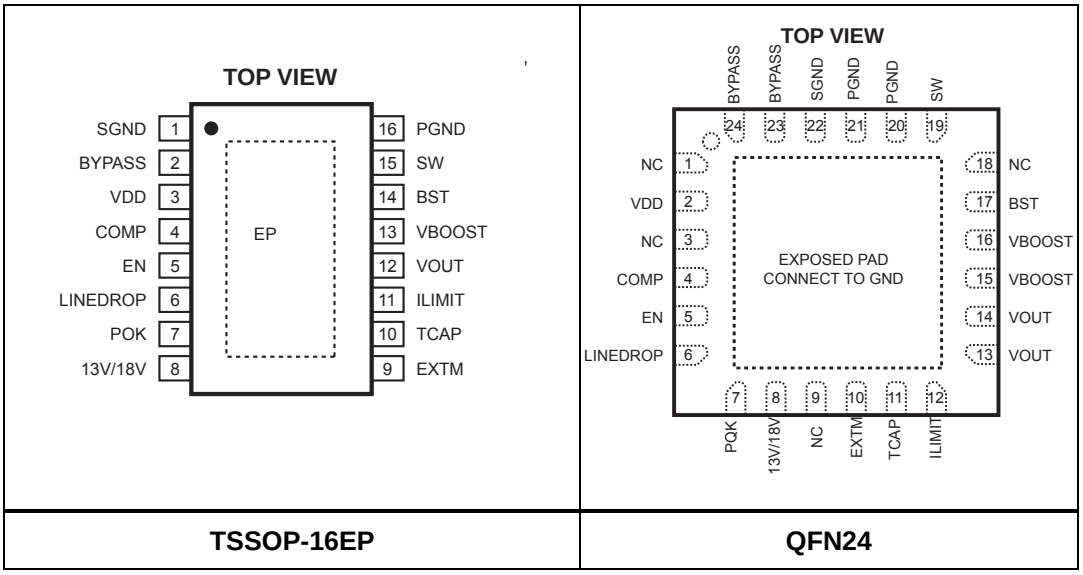


ORDERING INFORMATION

Part Number	Package	Top Marking
MP8126DF*	TSSOP16EP	MP8126
MP8126DR**	QFN24 (4X4mm)	MP8126

* For Tape & Reel, add suffix –Z (e.g. MP8126DF–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP8126DF–LF–Z)
** For Tape & Reel, add suffix –Z (e.g. MP8126DR–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP8126DR–LF–Z)

PACKAGE REFERENCE



TSSOP-16EP | **QFN24**

ABSOLUTE MAXIMUM RATINGS (1)

VDD .....-0.3V to 16V
VOUT, SW, VBOOST .....-0.3V to 25V
BST ..... V_{Boost} +7V
All Other Pins .....-0.3V to 6.5 V
Continuous Power Dissipation…..(T_A=+25°C) (2)
TSSOP-16EP……2.8W
QFN24(4x4mm)……2.9W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply Voltage VIN.....8V to 14V
Output Voltage VOUT 13V/14V/18V/19V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
TSSOP-16EP	45	8	°C/W
QFN24(4x4mm)	42	9	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer PCB

ELECTRICAL CHARACTERISTICS

VIN = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
General						
Input Voltage Range	VIN		8	12	14	V
Input Supply Current (5)	I_{IN}	EN=High, no load		5		mA
Under-Voltage Lockout	UVLO	VIN rising	7		8	V
UVLO Hysteresis				350		mV
EN Input Logic Threshold	V_{EN_High}	V_{EN} rising			2	V
	V_{EN_Low}	V_{EN} falling	0.8			V
13V/18V Input Logic Threshold	$V_{13/18\_High}$	$V_{13V/18V}$ rising			2	V
	$V_{13/18\_Low}$	$V_{13V/18V}$ falling	0.8			V
LINEDROP Input Logic Threshold	V_{LD_High}	$V_{LINEDROP}$ rising			2	V
	V_{LD_Low}	$V_{LINEDROP}$ falling	0.8			V
TCAP Pin Current	I_{CHA}	TCAP capacitor charging		7		µA
Output Backward Leakage Current (6)	I_{BKLK}	EN=Low, VOUT is clamped to 24V, VBOOST is floating		0.7	1	mA
Voltage on BYPASS pin	V_{BYP}			5		V
SWITCHING REGULATOR						
Boost Switch-On Resistance (5)	R_{DSON}	I_{OUT} =500mA		500		mΩ
Boost Frequency				342		kHz
LINEAR REGULATOR						
Dropout Voltage (5)		V_{BOOST}-VOUT, I_{OUT}=500mA		1.26		V
OUTPUT						
Output Voltage	VOUT	LINEDROP=Low, 13V/18V=Low, I_{OUT} =0-100mA	12.93	13.37	13.81	V
		LINEDROP=Low, 13V/18V=High, I_{OUT} =0-100mA	17.9	18.49	19.08	V
		LINEDROP=High, 13V/18V=Low, I_{OUT} =0-100mA	13.97	14.41	14. 85	V
		LINEDROP=High, 13V/18V=High, I_{OUT} =0-100mA	18.9 3	19.52	20.11	V
Output Line Regulation		8V≤VIN≤14V; I_{OUT}=100mA		4	40	mV
Output Load Regulation (5)		10mA≤I_{OUT}≤500mA, 13V/18V=Low		20		mV
		10mA≤I_{OUT}≤500mA, 13V/18V=High		30		mV

ELECTRICAL CHARACTERISTICS (*continued*)

VIN = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
TONE Signal						
EXTM Input Logic Threshold	V_{EXTM_High}	V_{EXTM} rising			2	V
	V_{EXTM_Low}	V_{EXTM} falling	0.8			V
EXTM Frequency Range (7)		V_{EXTM_High}=3.3V, V_{EXTM_Low}=0V	20	22	24	kHz
Peak-to-Peak Amplitude	V_{PP}	I_{OUT} = 0 to 100mA	0.4	0.6	0.8	V
Duty Cycle		R_L=1kΩ, C_L=0.1µF		50		%
Rise and Fall Time		R_L=1kΩ, C_L=0.1µF		8		µs
Over-Current Protection						
Output Current Limit	I_{LIMIT}	R_{LIMIT}=10kΩ	600	770	1100	mA
Dynamic Overload-Protection Off Time	t_{OFF}	Time between restart attempts		2		s
Dynamic Overload-Protection On Time	t_{ON}	Time to onset of shutdown		50		ms
POK						
POK Upper-Trip Threshold (5)		V_{FB} with respect to nominal		12		%
POK Lower-Trip Threshold		V_{FB} with respect to nominal		-12		%
POK Output Lower Voltage		I_{SINK} = 5mA			0.3	V
Thermal Protection						
Over-Temperature Shutdown (5)				150		°C
Over-Temperature Protection Hysteresis				20		°C

Notes:

5) Guaranteed by design.
6) Shall withstand the back voltage for an indefinite period of time. On removal of the fault condition the device returns to normal operation
7) This range is used to guarantee EXTM function.

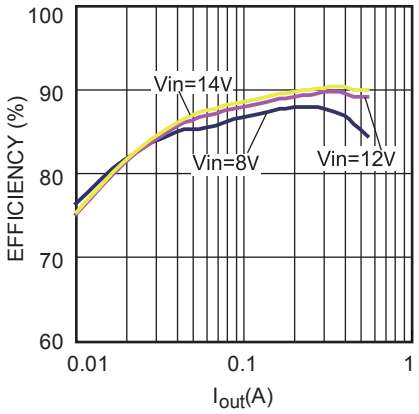
PIN FUNCTIONS

Pin # TSSOP-16	Pin # QFN24	Name	Description
1	22	SGND	Analog ground.
2	23, 24	BYPASS	Connect a bypass capacitor for the internal regulator.
3	2	VDD	Input supply.
4	4	COMP	Compensation pin for Boost regulator (47nF& 4.7k & 470pF is suggested).
5	5	EN	Regulator On/Off Control Input. The output is disabled when this pin goes low. The converter turns on when this pin goes high. Connect EN to the input source (through a 100kΩ pull-up resistor if VIN > 6V) for automatic startup. Do not leave EN floating.
6	6	LINEDROP	VOUT compensation selection. For voltage drops on the long coaxial cable. The LDO output increases by 1V when LINEDROP is high,. Do not leave LINEDROP floating.
7	7	POK	Power OK. A high output indicates that LDO output is within ±12% of nominal value. A low output means that LDO output is outside this window.
8	8	13V/18V	Select 13V or 18V. For output voltage. Select logic HIGH for 18V and LOW for 13V. Do not leave this pin floating.
9	10	EXTM	External Modulation Input. For 22kHz signaling that is internally shaped and transferred to the output. Tie it to ground if not used.
10	11	TCAP	Internal voltage reference for LDO output, A soft-start capacitor can be connected to this pin to set rise time of the output voltage. The capacitor should be very close to this pin and SGND, and the route should keeps far away from any noise like SW copper.
11	12	ILIMIT	Output Current Limit Set. Sets the LDO output current limit of LDO. Program using a resistor from ILIMIT to GND.
12	13, 14	VOUT	Output Voltage.
13	15, 16	VBOOST	Internal LDO Input.
14	17	BST	Internal LDO Driver Supply.
15	19	SW	Switching Input. Drain of the internal boost-stage MOSFET. Connect the power inductor and output rectifier to SW.
16	20, 21	PGND	Power Ground.
	1, 3, 9, 18	NC	Not Connect.
EP		Exposed Pad	Heatsink. Not connected internally. Connect to a metal GND pad for best results. Do not connect to other pins.

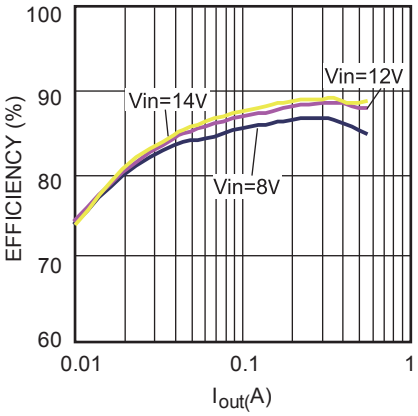
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the DESIGN EXAMPLE section.
VIN =12V, $V_{LINEDROP}$=5V, V_{EXTM}=0V, T_A = +25ºC, unless otherwise noted.

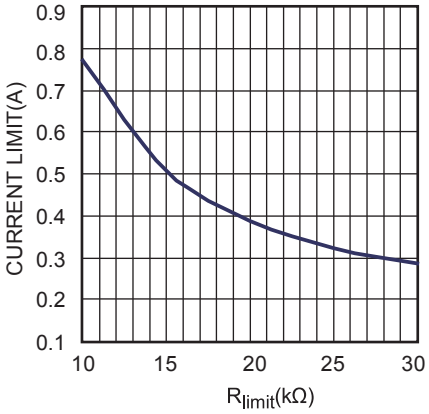
Efficiency for 19V output



Efficiency for 14V output



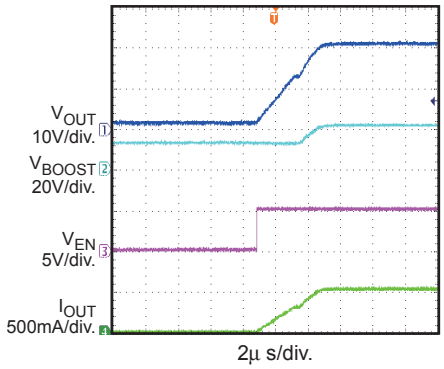
Current Limit vs. Rlimit



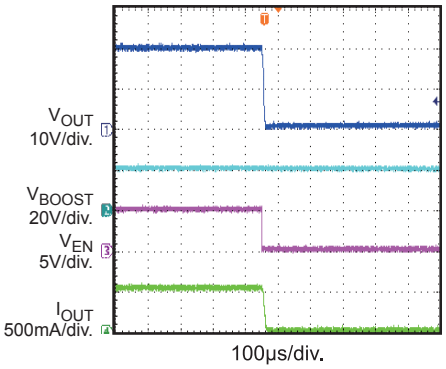
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the DESIGN EXAMPLE section.
VIN =12V, $V_{LINEDROP}$=5V, V_{EXTM}=0V, IOUT=0.55A, T_A = +25ºC, unless otherwise noted.

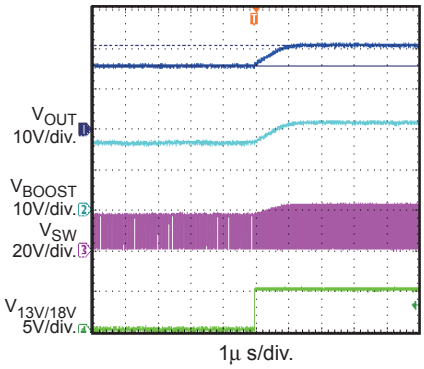
EN Startup



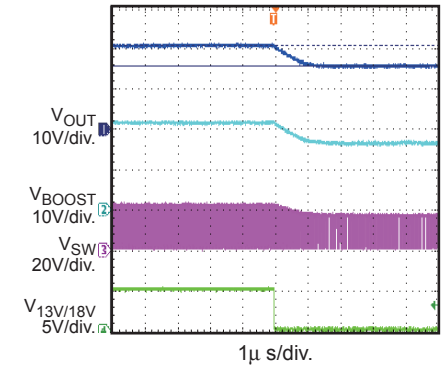
EN Shutdown



13V to 18V Switch

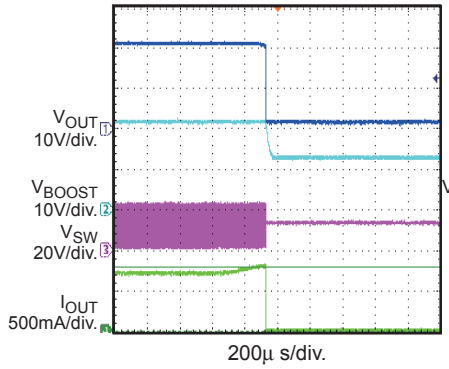


18V to 13V Switch



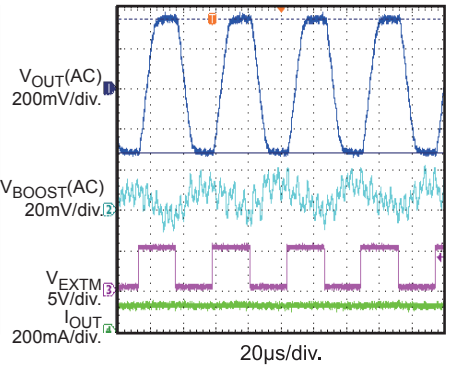
Current Limit Protection

R_{LIMIT} = 10kΩ



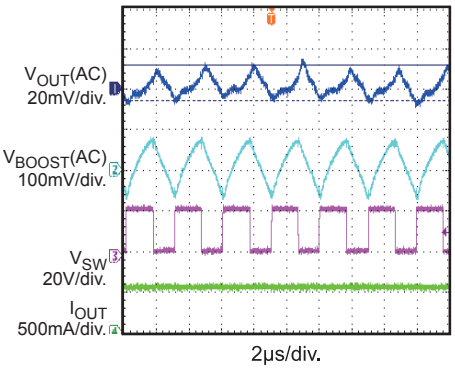
22kHz Tone Signal

Vin=12V, Vo=19V,Io=0.1A



Output Ripple

Vin=12V, Vo=19V,Io=0.55A



BLOCK DIAGRAM

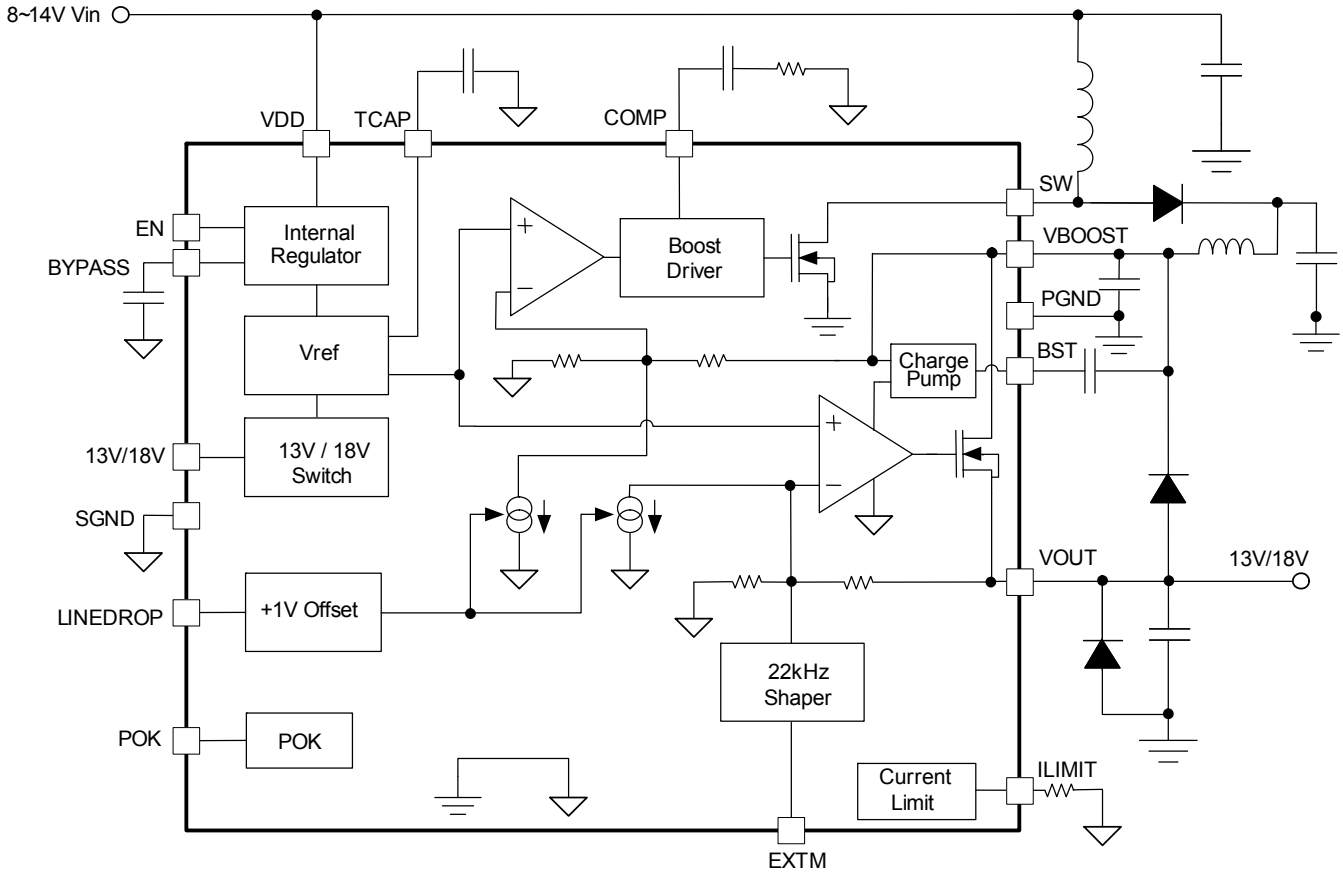


Figure 1: Functional Block Diagram

OPERATION

The MP8126 is a single-output voltage regulator that provides both the supply voltage and the control signal from satellite set-top box modules to the LNB (low noise block) of the antenna port.

The MP8126 has an integrated boost converter that—from a single supply source between 8V and 14V—generates a voltage that enables the linear post-regulator to function while minimizing power dissipation.

Boost Converter/Linear Regulator

The boost converter is a fixed-frequency, non-synchronous, voltage regulator with peak current mode control. The operating frequency is 342 kHz, typically.

To reduce power dissipation, the boost converter operates in a pulse-skipping mode at light load.

The output voltage of the boost converter tracks the requested output voltage to allow the linear regulator to work at the minimum drop-out voltage.

13V/18V Switching

The 13V/18V logic input pin can set the output voltage to select different LNB polarization directions. A logic HIGH sets the output to 18V LOW sets it to 13V.

LINEDROP Control

The MP8126 has a voltage compensation function that compensates for excessive voltage drop along the coaxial cable. Setting the LINEDROP pin to HIGH allows the output voltage increases by 1V while LOW disables the function.

Soft-Start

An external capacitor (C_{SS}) implements the soft-start function. Estimate the value of C_{SS} given the required slew rate (k) of the output voltage using the following formula:

$$C_{SS} = (15 \times I_{CHA}) / k$$

Where I_{CHA} is typically 7μA.

Current Limit

An external resistor connected to the I_{LIMIT} pin limits the output current dynamically. Select R_{LIMIT} using the following formula:

$$I_{LIMIT} = 7700 / R_{LIMIT}$$

When an overload occurs, the device regulates the output current at the current limit level for 50ms. If the overload is still detected after this 50ms, the output shuts down for 2 seconds before the resuming the output.

The boost converter uses an integrated cycle-by-cycle over-current limit function that guarantees the part works with a full load.

To ensure normal current-limiting functionality, select a R_{LIMIT} not less than 10kΩ

Power Good (POK)

POK connects to an internal, open-drain device. When the output voltage falls out of the ±12% normal value range, POK is pulled down. Otherwise, POK is pulled high.

Tone Generation

In accordance with DiSEqC standards, the part can detect a 22kHz signal through EXTM pin, shape it with the built-in amplitudes and rise/fall times, and modulate the output (Figure 2). Tie the EXTM pin to GND if the 22kHz signal isn't needed.

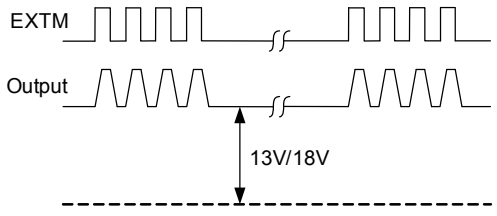


Figure 2: Tone Signal at Output

Thermal Protection

When the junction temperature exceeds +150°C, the part shuts down. Once the junction temperature cools—typically to 130°C—the part restarts automatically.

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Input Capacitor

The input capacitor (C1) is required to maintain the DC input voltage. For best results, use ceramic capacitors with low ESR/ESL. Estimate the input voltage ripple using the formula below:

$$\Delta V_{IN} = \frac{V_{IN}}{8f_s^2 \cdot L \cdot C1} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

A 10μF X7R ceramic capacitor is recommended for most application.

Setting the Output Boost Converter Capacitor

The output current of the step-up converter is discontinuous, and therefore requires a capacitor to supply the AC current to the load. Use low-ESR capacitors for the best performance. The output voltage ripple can be estimated by the below formula.

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot R_L \cdot C2} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

Where R_L is the value of load resistor.

Ceramic capacitors with X7R dielectrics are highly recommended because of their low ESR and small temperature coefficient. Typically, a 22μF X7R ceramic capacitor is recommended.

Selecting the Inductor of Boost Converter

Select an inductor with a DC current rating that is at least 25% higher than the maximum load current. For most designs, derive the inductance value from the following equation.

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{f_s \cdot V_{OUT} \cdot \Delta I_L}$$

Where ΔI_L is the inductor ripple current. Choose the inductor ripple current to be approximately 30% of the maximum load current.

Selecting the Boost Converter Rectifier Diode

The high switching frequency requires high-speed rectifiers, such as Schottky diodes for their fast recovery times and low forward voltage. For most applications, use a 2A Schottky diode.

DESIGN EXAMPLE

Below is a design example that follows the application guidelines for the following specifications:

V_{IN}	12V
V_{OUT}	19V

Figure 4 shows the detailed application schematic. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more applications, please refer to the Evaluation Board Data Sheet.

LAYOUT RECOMMENDATION

Layout is important, poor layout results in reduced performance, EMI problems, resistive loss, and even system instability. Following the below rules and figure 3 for the layout design:

1. Place high current path(SW, D1, C2 and IC-PGND) very close to the device with short, direct and wide traces.
2. Place the decoupling capacitor C3 across VDD and SGND as close as possible.
3. Place the decoupling capacitor C4 across BYPASS and SGND as close as possible.
4. Place the LDO input/output capacitor C11/C8 across VBOOST/VOUT and PGND as close as possible.
5. Place capacitor C7 across TCAP and SGND pins as close as possible.
6. Keep the switching node (SW) plane as small as possible and far away from the TCAP and ILIMT trace.
7. Add copper and vias on GND net around the device to help dissipate heat. The PGND and SGND should be connected through a star ground.

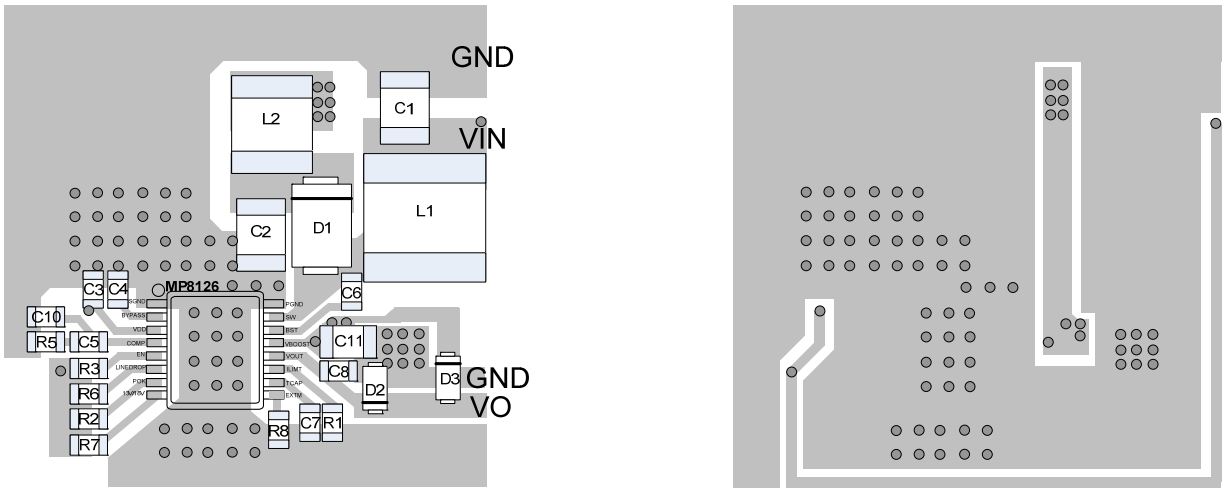


Figure 3: MP8126DF PCB Layout Guide

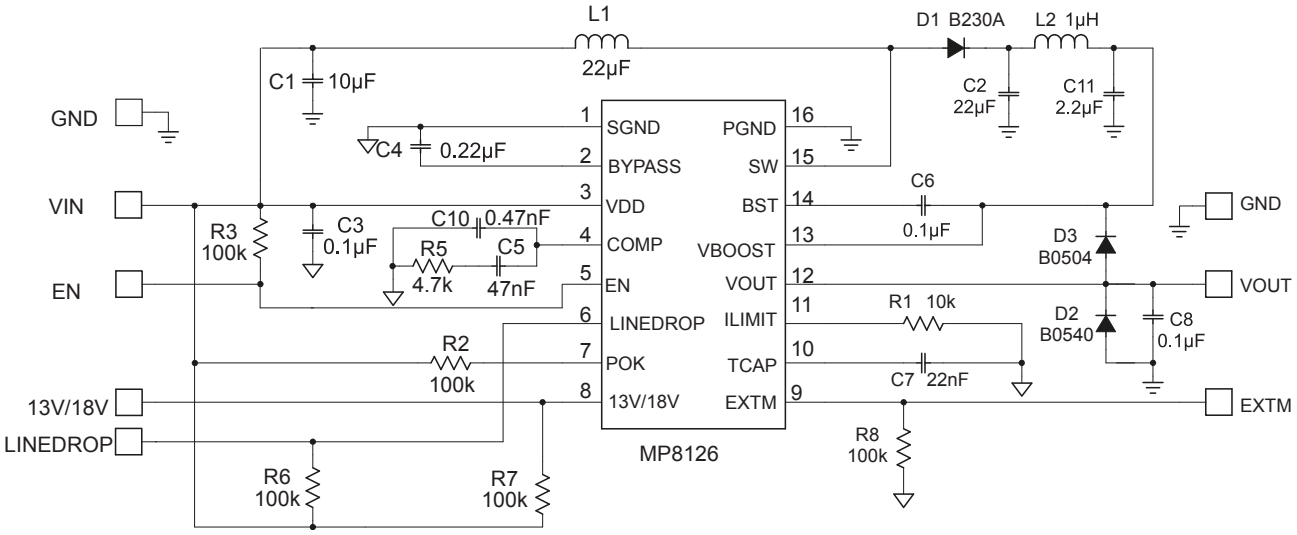
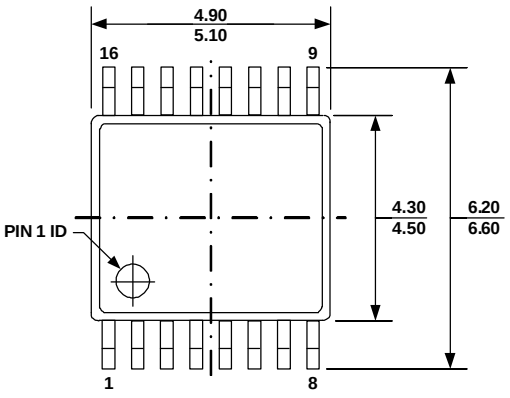


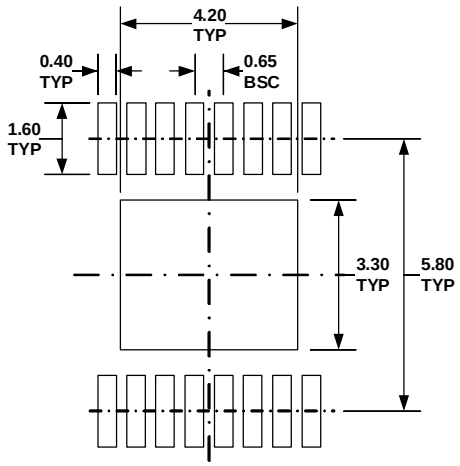
Figure 4: Detailed Application Schematic

PACKAGE INFORMATION

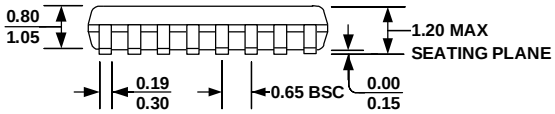
TSSOP16EP



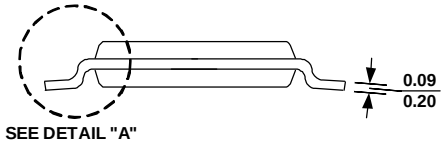
TOP VIEW



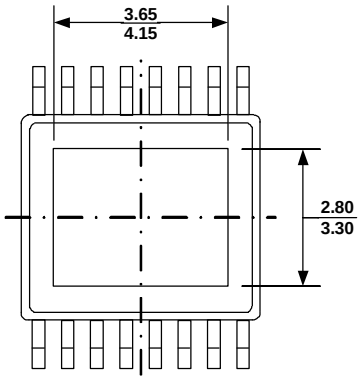
RECOMMENDED LAND PATTERN



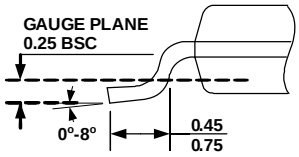
FRONT VIEW



SIDE VIEW



BOTTOM VIEW

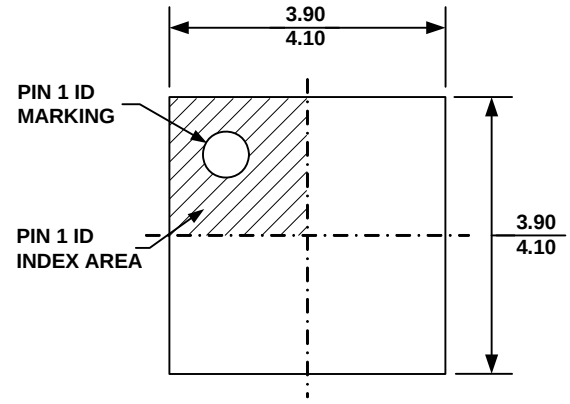


DETAIL "A"

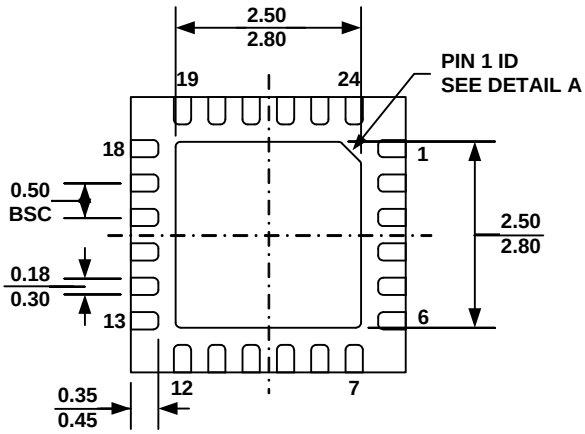
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
6) DRAWING IS NOT TO SCALE

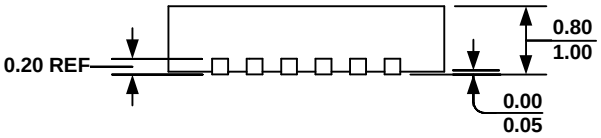
QFN24 (4X4mm)



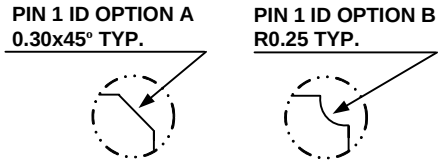
TOP VIEW



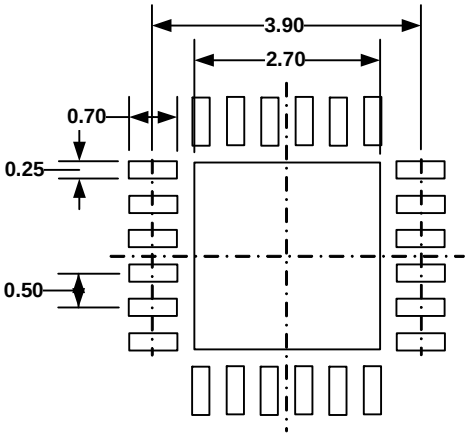
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION VGGD.
5) DRAWING IS NOT TO SCALE.