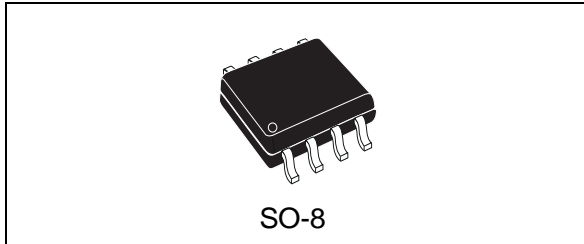


OMNIFET III fully protected low-side driver

Datasheet - production data



Description

The VNLD5090-E is a monolithic device made using STMicroelectronics® VIPower® technology, intended for driving resistive or inductive loads with one side connected to the battery. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. Output current limitation protects the device in an overload condition. In case of long duration overload, the device limits the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown, with automatic restart, allows the device to recover normal operation as soon as a fault condition disappears. Fast demagnetization of inductive loads is achieved at turn-off.

Features

Type	V _{clamp}	R _{DS(on)}	I _D
VNLD5090-E	41 V	90 mΩ	25 A

- Automotive qualified
- Drain current: 13 A
- ESD protection
- Overvoltage clamp
- Thermal shutdown
- Current and power limitation
- Very low standby current
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC European directive
- Open drain status output

Table 1. Devices summary

Package	Order codes	
	Tube	Tape and reel
SO-8	VNLD5090-E	VNLD5090TR-E

Contents

- 1 Block diagrams and pins configurations 5**
- 2 Electical specifications 7**
 - 2.1 Absolute maximum ratings 7
 - 2.2 Thermal data 7
 - 2.3 Electrical characteristics 8
- 3 Application information 11**
 - 3.1 MCU I/O protection 11
- 4 Package and PC board thermal data 13**
 - 4.1 SO-8 thermal data 13
- 5 Package and packing information 16**
 - 5.1 ECOPACK® 16
 - 5.2 SO-8 mechanical data 16
 - 5.3 SO-8 packing information 18
- 6 Revision history 19**

List of tables

Table 1.	Devices summary	1
Table 2.	Pin function	5
Table 3.	Suggested connections for unused and n.c. pins	6
Table 4.	Absolute maximum ratings	7
Table 5.	Thermal data	7
Table 6.	PowerMOS section	8
Table 7.	Source drain diode	8
Table 8.	Input section	8
Table 9.	Status pin	8
Table 10.	Switching characteristics	9
Table 11.	Protection and diagnostics	9
Table 12.	Truth table.	10
Table 13.	SO-8 thermal parameters	15
Table 14.	SO-8 mechanical data	17
Table 15.	Document revision history	19

List of figures

Figure 1.	Block diagram	5
Figure 2.	Current and voltage conventions	6
Figure 3.	Configuration diagrams (top view)	6
Figure 4.	Switching characteristics	10
Figure 5.	Application schematic	11
Figure 6.	Maximum demagnetization energy ($V_{CC} = 16\text{ V}$)	12
Figure 7.	SO-8 PC board	13
Figure 8.	SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air condition	13
Figure 9.	SO-8 thermal impedance junction ambient single pulse	14
Figure 10.	Thermal fitting model of a LSD in SO-8	14
Figure 11.	SO-8 package dimensions	16
Figure 12.	SO-8 tube shipment (no suffix)	18
Figure 13.	SO-8 tape and reel shipment (suffix "TR")	18

1 Block diagrams and pins configurations

Figure 1. Block diagram

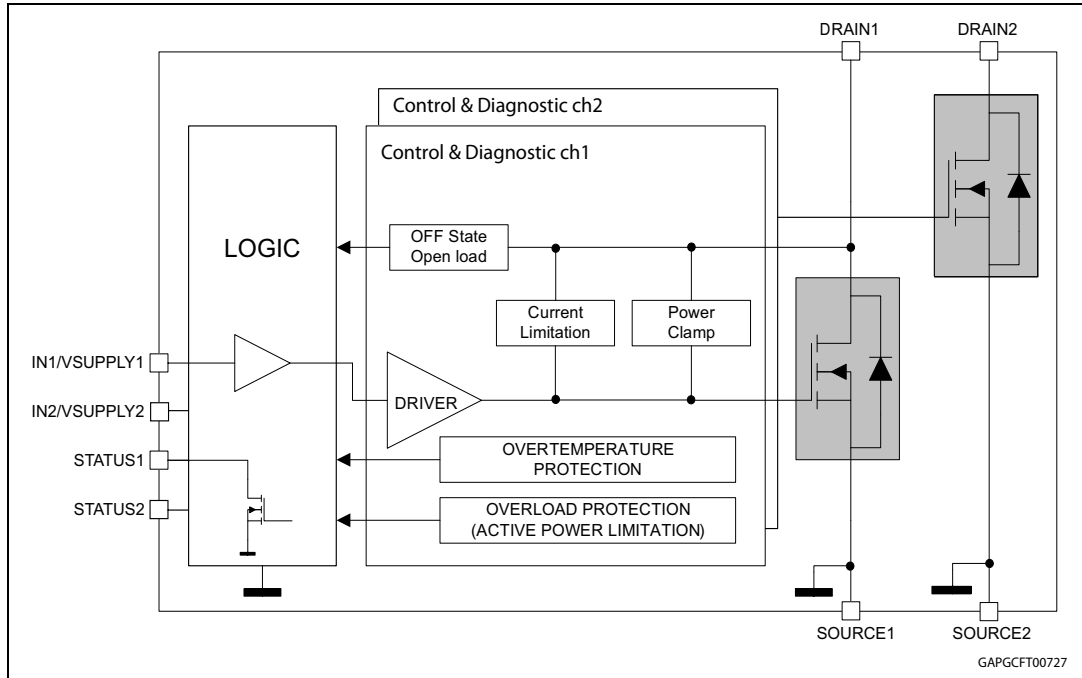


Table 2. Pin function

Name	Function
IN _{1,2} /VSUPPLY _{1,2}	Voltage controlled input pin with hysteresis, CMOS compatible. They controls output switch state
DRAIN _{1,2}	PowerMOS drain
SOURCE _{1,2}	PowerMOS source and ground reference for the control section
STATUS _{1,2}	Open drain digital diagnostic pin

Figure 2. Current and voltage conventions

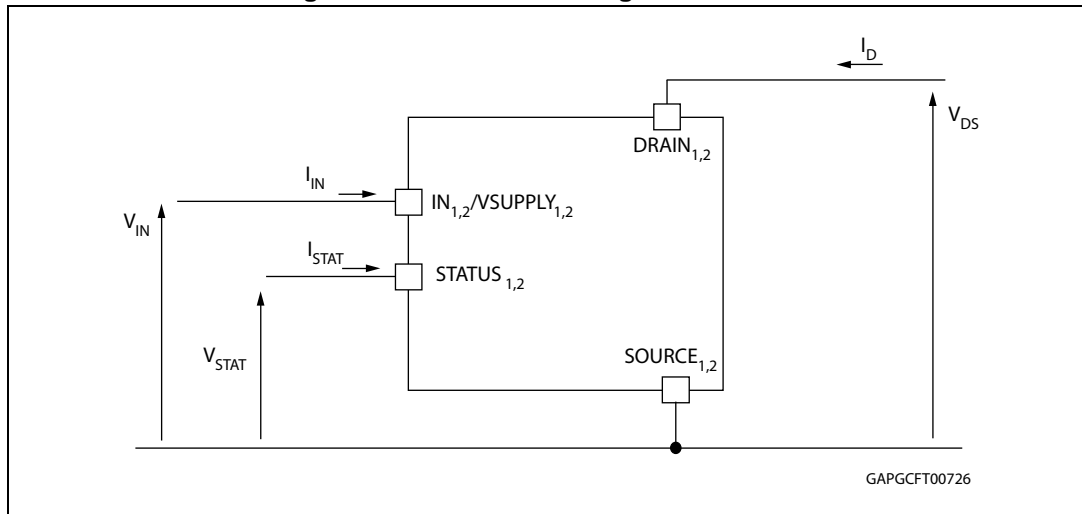


Figure 3. Configuration diagrams (top view)

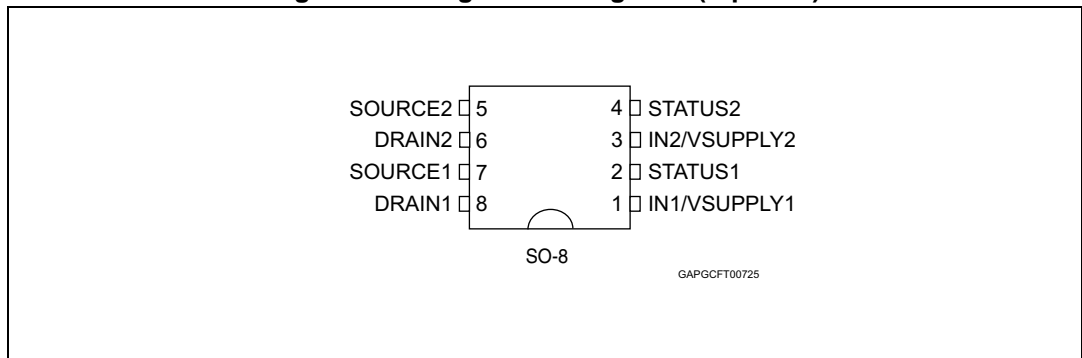


Table 3. Suggested connections for unused and n.c. pins

Connection / pin	STATUS _{1,2}	N.C.	INPUT _{1,2}
Floating	X ⁽¹⁾	X	X
To ground	Not allowed	X	Through 10 kΩ resistor

1. X: do not care.

2 Electical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
		SO-8	
V_{DS}	Drain-source voltage ($V_{IN} = 0$ V)	Internally clamped	V
I_D	DC drain current	Internally limited	A
$-I_D$	Reverse DC drain current	12.5	A
I_S	DC supply current	-1 to 10	mA
I_{IN}	DC input current	-1 to 10	mA
I_{STAT}	DC status current	-1 to 10	mA
V_{ESD1}	Electrostatic discharge ($R = 1.5$ k Ω ; $C = 100$ pF) – DRAIN – SUPPLY, INPUT, STATUS	5000 4000	V
V_{ESD2}	Electrostatic discharge on output pin only ($R = 330$ Ω , $C = 150$ pF)	2000	V
T_j	Junction operating temperature	-40 to 150	$^{\circ}$ C
T_{stg}	Storage temperature	-55 to 150	$^{\circ}$ C
E_{AS}	Single pulse avalanche energy ($L = 1.1$ mH; $T_j = 150$ $^{\circ}$ C; $R_L = 0$; $I_{OUT} = I_{limL}$)	50	mJ

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Maximum value	Unit
		SO-8	
$R_{thj-amb}$	Thermal resistance junction-ambient	108	$^{\circ}$ C/W

2.3 Electrical characteristics

Values specified in this section are for $V_{INx/SUPPLYx} = 4.5\text{ V to }5.5\text{ V}$, $-40^{\circ}\text{C} < T_j < 150^{\circ}\text{C}$, unless otherwise stated.

Table 6. PowerMOS section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON}	ON-state resistance	$I_D = 1.6\text{ A}$; $T_j = 25^{\circ}\text{C}$, $V_{INx/SUPPLYx} = 5\text{ V}$			90	m Ω
		$I_D = 1.6\text{ A}$; $T_j = 150^{\circ}\text{C}$, $V_{INx/SUPPLYx} = 5\text{ V}$			180	
		$I_D = 1.6\text{ A}$; $T_j = 150^{\circ}\text{C}$, $V_{INx/SUPPLYx} = 4.5\text{ V}$			190	
V_{CLAMP}	Drain-source clamp voltage	$V_{IN} = 5\text{ V}$; $I_D = 1.6\text{ A}$	41	46	52	V
V_{CLTH}	Drain-source clamp threshold voltage	$V_{IN} = 0\text{ V}$; $I_D = 2\text{ mA}$	36			V
I_{DSS}	OFF-state output current	$V_{IN} = 0\text{ V}$; $V_{DS} = 13\text{ V}$; $T_j = 25^{\circ}\text{C}$	0		3	μA
		$V_{IN} = 0\text{ V}$; $V_{DS} = 13\text{ V}$; $T_j = 125^{\circ}\text{C}$	0		5	

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	$I_D = 1.6\text{ A}$; $V_{IN} = 0\text{ V}$	—	0.8	—	V

Table 8. Input section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{ISS}	Supply current from input pin	ON-state: $V_{INx/SUPPLYx} = 5\text{ V}$; $V_{DS} = 0\text{ V}$		30	65	μA
		OFF-state; $T_j = 25^{\circ}\text{C}$; $V_{IN} = V_{DRAIN} = 0\text{ V}$;		10	25	
V_{ICL}	Input clamp voltage	$I_S = 1\text{ mA}$	5.5		7	V
		$I_S = -1\text{ mA}$		-0.7		
V_{INTH}	Input threshold voltage	$V_{DS} = V_{IN}$; $I_D = 1\text{ mA}$	1		3.5	V

Table 9. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1\text{ mA}$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = 5\text{ V}$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5\text{ V}$			100	pF

Table 9. Status pin (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{STCL}	Status clamp voltage	I _{STAT} = 1 mA	5.5		7	V
		I _{STAT} = -1 mA		-0.7		

Table 10. Switching characteristics⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(ON)}	Turn-on delay time	R _L = 8.2 Ω; V _{CC} = 13 V ⁽²⁾	—	8	—	μs
t _{d(OFF)}	Turn-off delay time	R _L = 8.2 Ω; V _{CC} = 13 V ⁽²⁾	—	3.4	—	μs
t _r	Rise time	R _L = 8.2 Ω; V _{CC} = 13 V ⁽²⁾	—	10	—	μs
t _f	Fall time	R _L = 8.2 Ω; V _{CC} = 13 V ⁽²⁾	—	2.7	—	μs
W _{ON}	Switching energy losses at turn-on	R _L = 8.2 Ω; V _{CC} = 13 V ⁽²⁾	—	57	—	μJ
W _{OFF}	Switching energy losses at turn-off	R _L = 8.2 Ω; V _{CC} = 13 V ⁽²⁾	—	14	—	μJ
Qg	Total gate charge	V _{INx/SUPPLYx} = 5 V		2		nC

1. See [Figure 5: Application schematic](#).
2. See [Figure 4: Switching characteristics](#).

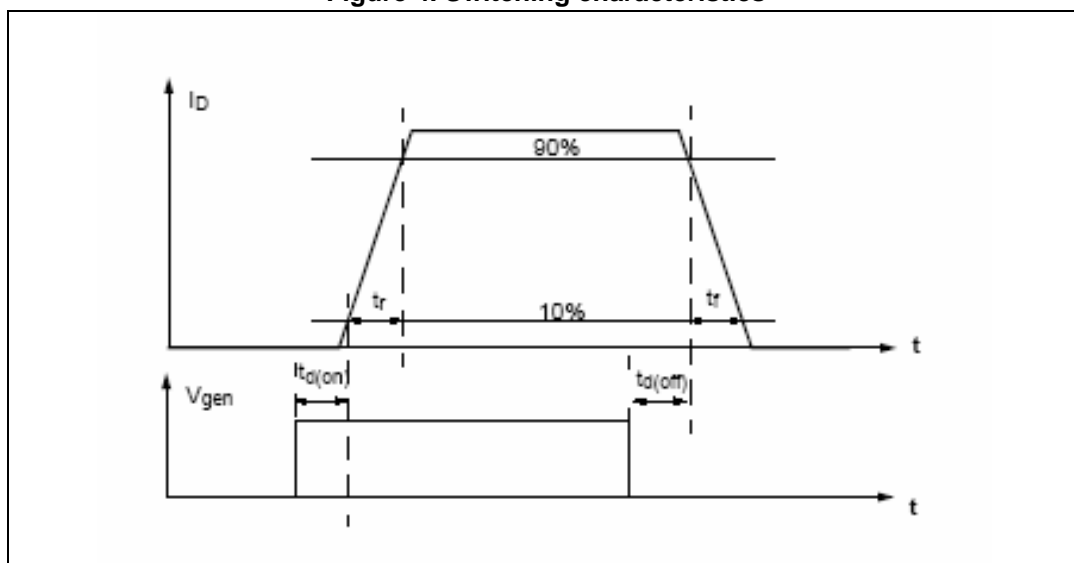
Table 11. Protection and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{limH}	DC short-circuit current	V _{DS} = 13 V; V _{INx/SUPPLYx} = 5 V	13	18	25	A
I _{limL}	Short-circuit current during thermal cycling	V _{DS} = 13 V; T _R < T _j < T _{TSD} ; V _{INx/SUPPLYx} = 5 V		8		A
t _{dimL}	Step response current limit	V _{DS} = 13 V; V _{input} = 5 V		44		μs
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature		T _{RS} + 1	T _{RS} + 5		°C
T _{RS}	Thermal reset of STATUS		135			°C
T _{HYST}	Thermal hysteresis (T _{TSD} - T _R)			7		°C

Table 12. Truth table

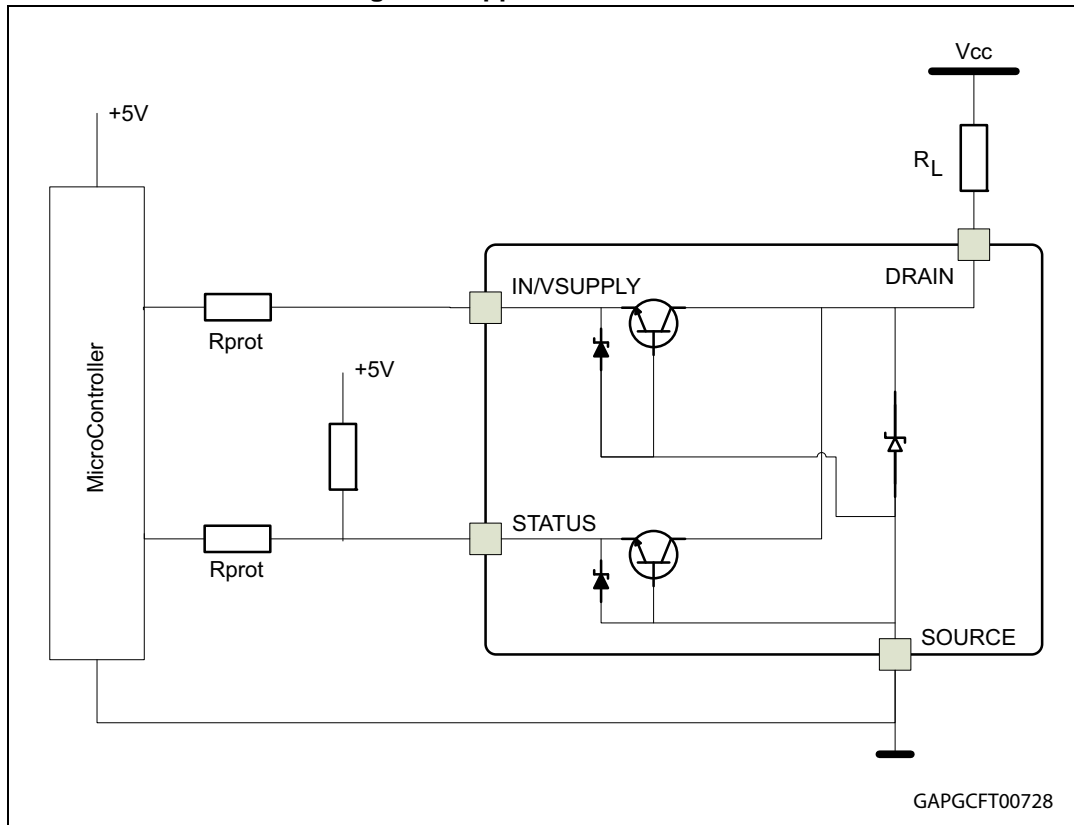
Conditions	INPUT	DRAIN	STATUS
Normal operation	L	H	H
	H	L	H
Current limitation	L	H	H
	H	X	H
Overtemperature	L	H	H
	H	H	L
Undervoltage	L	H	X
	H	H	X

Figure 4. Switching characteristics



3 Application information

Figure 5. Application schematic



3.1 MCU I/O protection

ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching up^(a). The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the LSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os:

Equation 1

$$\frac{0.7}{I_{latchup}} \leq R_{prot} \leq \frac{(V_{OH\mu C} - V_{IH})}{I_{IH\ max}}$$

Let:

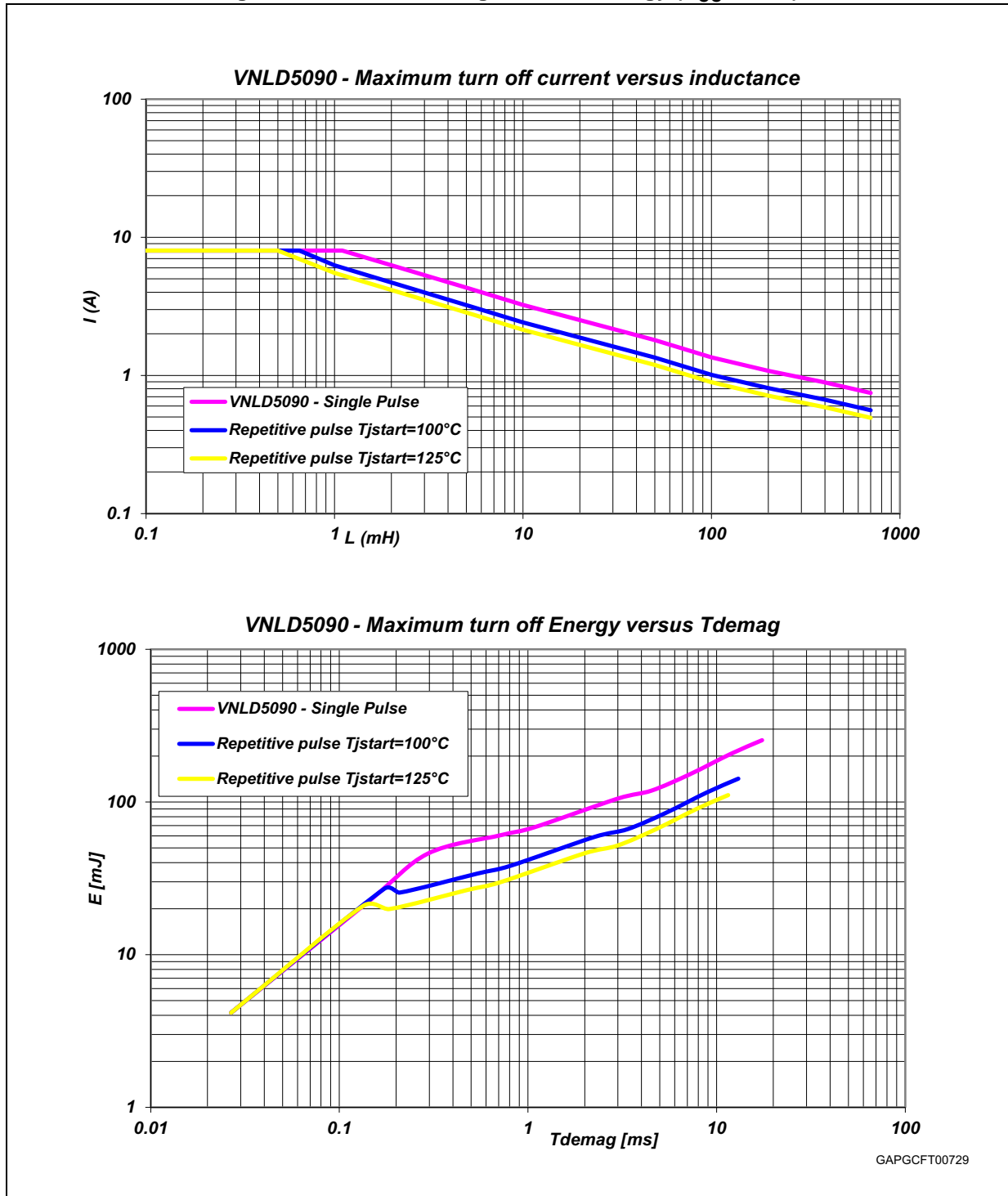
- $I_{latchup} \geq 20\ \text{mA}$
- $V_{OH\mu C} \geq 4.5\ \text{V}$
- $35\ \Omega \leq R_{prot} \leq 100\ \text{K}\Omega$

a. In case of negative transient on the drain pin.

Then, the recommended value is $R_{prot} = 1\text{ K}\Omega$

Figure 6 shows the turn-off current drawn during the demagnetization.

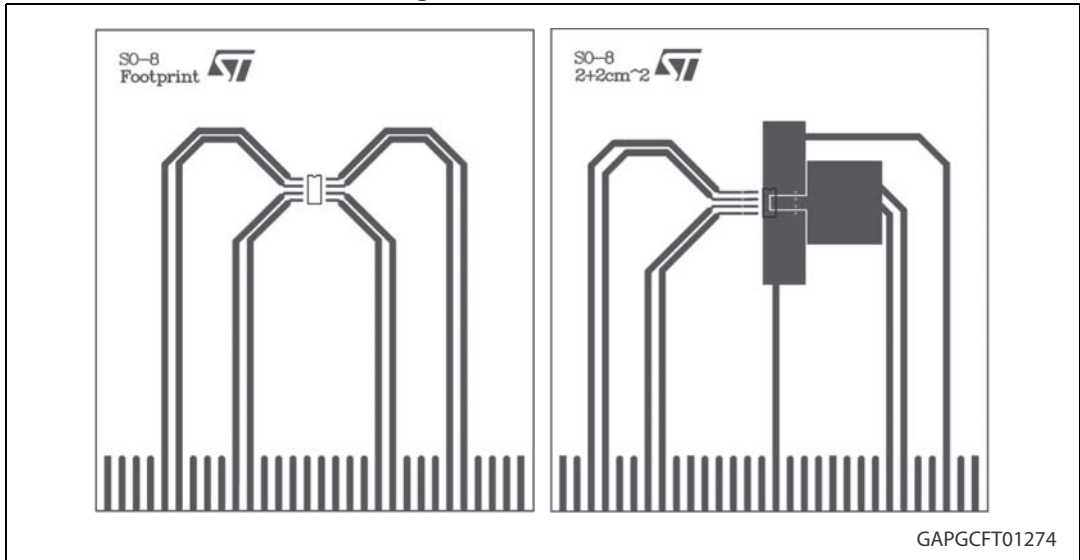
Figure 6. Maximum demagnetization energy ($V_{CC} = 16\text{ V}$)



4 Package and PC board thermal data

4.1 SO-8 thermal data

Figure 7. SO-8 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 78 mm x 86 mm; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal via separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm).

Figure 8. SO-8 $R_{thj-amb}$ vs PCB copper area in open box free air condition

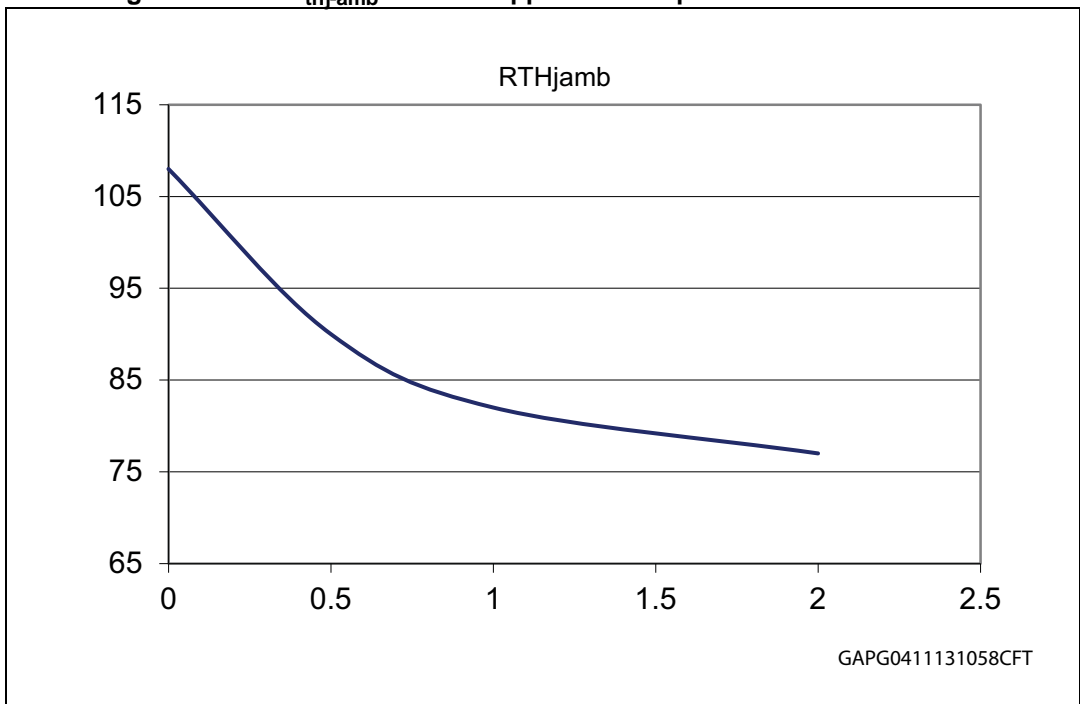
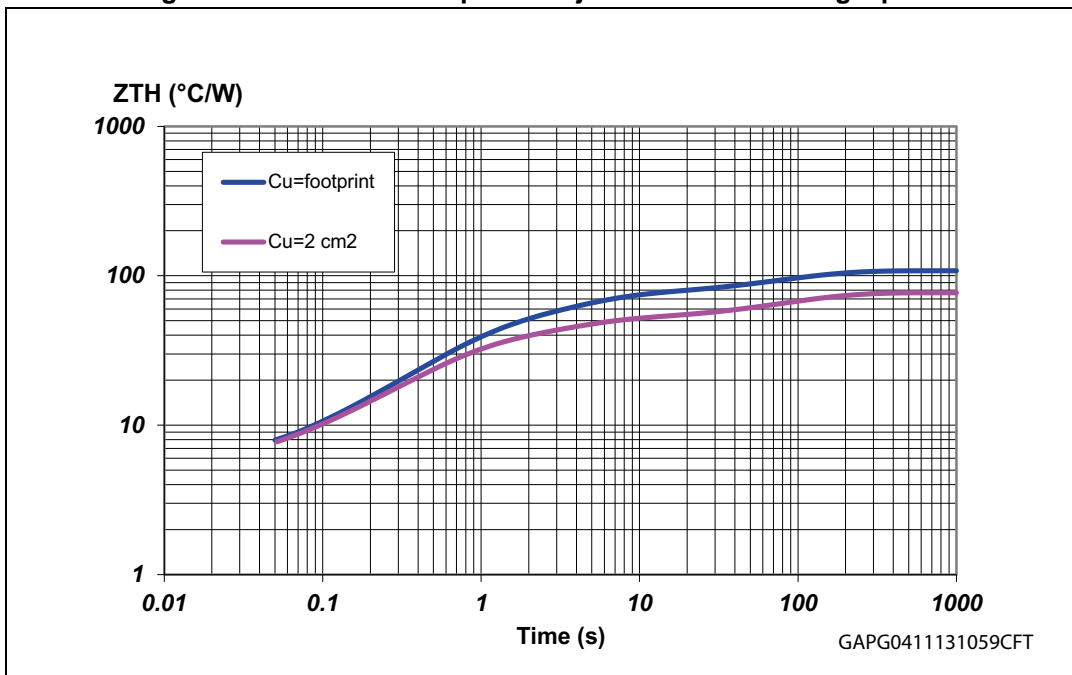


Figure 9. SO-8 thermal impedance junction ambient single pulse

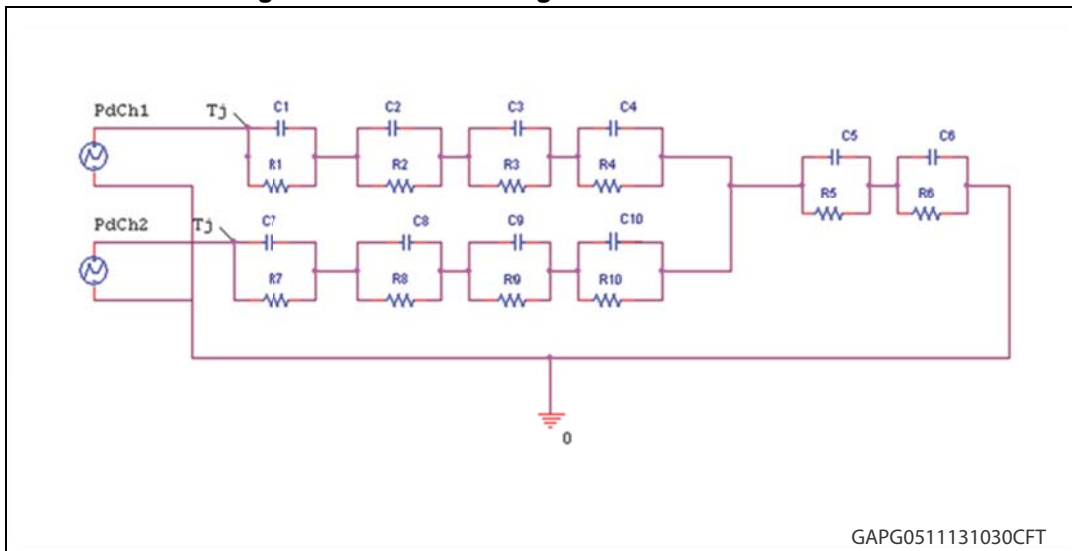


Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 10. Thermal fitting model of a LSD in SO-8



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 13. SO-8 thermal parameters

Area/island (cm ²)	Footprint	2
R1 = R7 (°C/W)	0.8	0.8
R2 = R8 (°C/W)	2.7	2.7
R3 = R9 (°C/W)	1.5	1.5
R4 = R10 (°C/W)	32	25
R5 (°C/W)	36	20
R6 (°C/W)	35	27
C1 = C7 (W.s/°C)	0.00005	0.00005
C2 = C8 (W.s/°C)	0.001	0.001
C3 = C9 (W.s/°C)	0.01	0.01
C4 = C10 (W.s/°C)	0.02	0.02
C5 (W.s/°C)	0.1	0.15
C6 (W.s/°C)	2.5	3.5

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 SO-8 mechanical data

Figure 11. SO-8 package dimensions

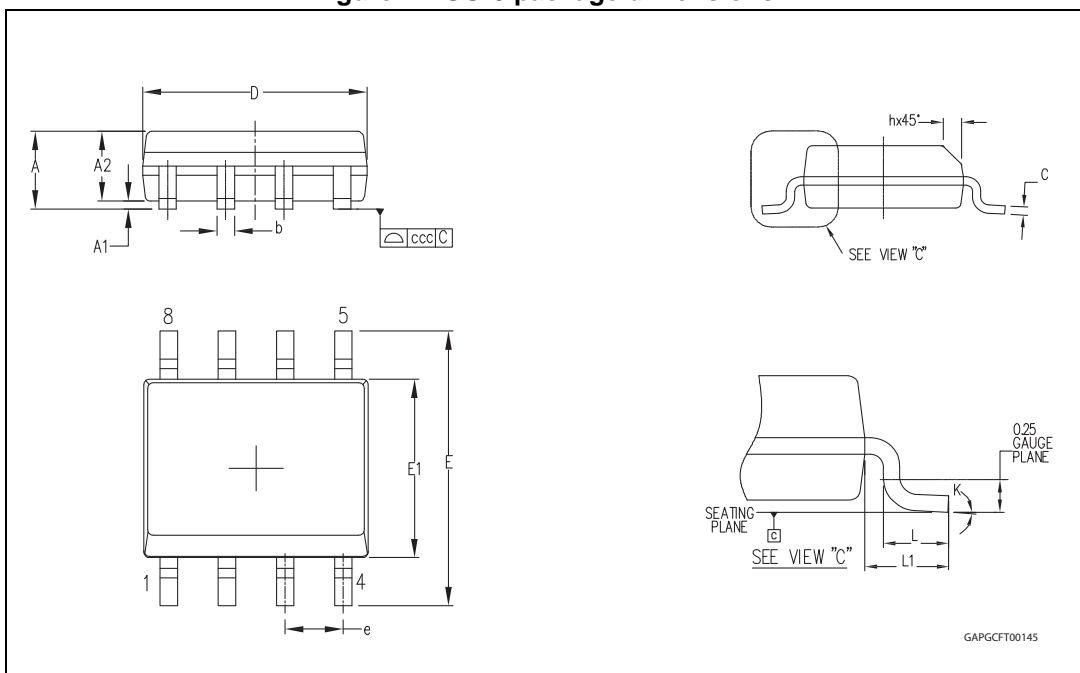


Table 14. SO-8 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D ⁽¹⁾	4.80	4.90	5.00
E	5.80	6.00	6.20
E1 ⁽²⁾	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total (both side).
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm per side.

5.3 SO-8 packing information

Figure 12. SO-8 tube shipment (no suffix)

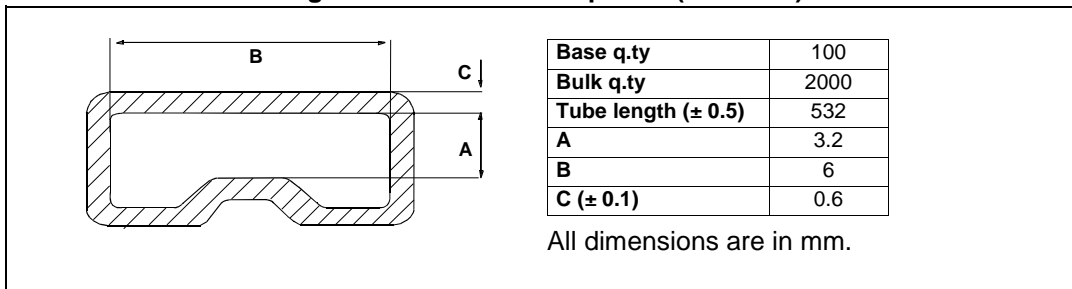
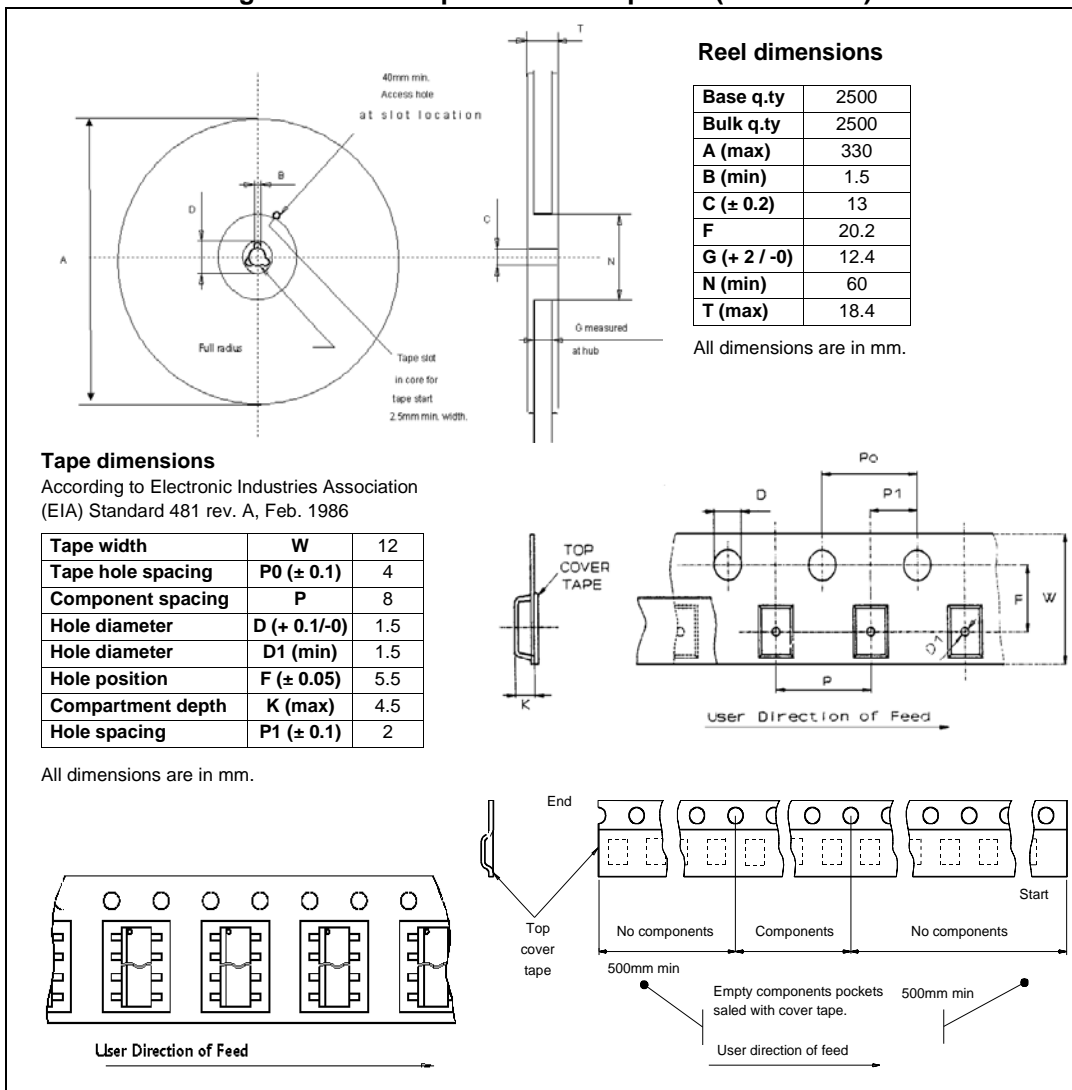


Figure 13. SO-8 tape and reel shipment (suffix "TR")



6 Revision history

Table 15. Document revision history

Date	Revision	Changes
16-May-2012	1	Initial release.
21-Jun-2012	2	Updated Figure 3: Configuration diagrams (top view)
13-Nov-2013	3	Updated Features list Updated Table 4: Absolute maximum ratings : – I_D , E_{AS} : updated values Updated Table 5: Thermal data Updated Table 6: PowerMOS section : – V_{CLAMP} : updated parameter Updated Table 8: Input section : – I_{SS} : updated maximum value Updated Table 10: Switching characteristics : – W_{ON} , W_{OFF} : updated unit values Updated Figure 5: Application schematic Updated Section 3.1: MCU I/O protection Added Chapter 4: Package and PC board thermal data
26-Feb-2015	4	Updated Table 12: Truth table : removed “Output voltage < V_{OL} ” condition

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